AKAI
SERVICE MANUAL

Model:

LCT2716

Safety Instructions
Features & Specifications
Block Diagram
Circuit Diagram
Disassembly
Schematic & Component Diagrams
Bill of Material
Pin Descriptions
LCD Panel specification
Exploded View Diagram

This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

I. Safety Instructions

CAUTION

RISK OF ELECTRIC SHOCK DO NOT OPEN

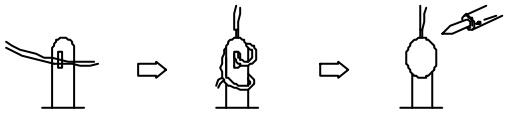
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated " dangerous voltage" within the product' s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

Before servicing this TV receiver, read the X-RAY RADIATION PRECAUTION, SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

X-RAY RADIATION PRECAUTION

1. Excessively high can produce potentially hazardous X-RAY RADIATION. To avoid such hazards, the high voltage must not exceed the specified limit. The normal value of the high voltage of this TV receiver is 27 KV at zero bean current (minimum brightness). The high voltage must not exceed 30 KV under any circumstances. Each time when a receiver requires servicing, the high voltage should be checked. The reading of the high voltage is recommended to be recorded as a part of the service record, It is important to use an accurate and reliable high voltage meter.
2. The only source of X-RAY RADIATION in this TV receiver is the picture tube. For continued X-RAY RADIATION protection, the replacement tube must be exactly the same type as specified in the parts list.
3. Some parts in this TV receiver have special safety related characteristics for X-RADIATION protection. For continued safety, the parts replacement should be under taken only after referring the PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

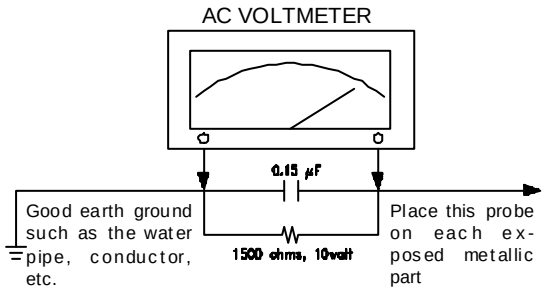
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15µF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time.

   Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

   The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.

1. FEATURES

- POWER SUPPLY	**: AC 90~264V 50/60Hz**
- MULTI TV SYSTEM	**: NTSC M**
- MULTISTANDARD SOUND PROCESSORS	**: BTSC+SAP**
- MULTI VEDEO SYSTEM	**: PAL/NTSC/SECAM**
VERSATILE INPUT SOURCE	**: TV, AV1, AV2, S- VIDEO,**
	YCbCr, YPbPr, DVI, PC(ANALOG)
- FULL FUNCTION REMOTE CONTROLLER	
EXCELLENT SOUND EFFECT WITH VOLUME,	
TRABLE, BASS, BALANCE, AVC ADJUSTABLE	
AUDIO MODE, SPACIAL EFFECT, EQUALIZER	
- SMART SOUND SET	**: PERSONAL,CINEMA, SPEECH, MUSIC,**
PICTURE MODE SET	**: STANDARD,PERSONAL, MILD ,BRIGHT,**
- ADAPTIVE 2/4 LINE COMB FILTER FOR PAL/NTSC	
- VTR FOR WEAK AND DISTORETED	
- SIGNAL FROM VIDEO TAPE RECORDER	
- AUTOMATICALLY TURN OFF THE SET WHEN	
- SIGNAL ABSENT LONGER THAN 10 MINUTES	
- 216 CHANNELS	
- BLUE SCREEN DISPLAY	
- / V-CHIP	
- FREEZE PICTURE	
- PROGRAM LABEL	
- SLEEP	
- SCREEN SIZE CHANGE	
- STANDBY	
- CHANNEL SWAP	
- VOG PIP (AT PC 1280X768/60Hz, TV WIDE FORMAT)	

GENERAL SPECIFICATIONS

ITEM	**DESCRIPTION**
-POWER CONSUMPTION	**180Watt（ MAX.）**
	≤3Watt(STBY)
-TV RECEIVE SYSTEM	**NTSC M**
-VIDEO SYSTEM	**PAL/ SECAM/ NTSC**
-VISION INTERMEDIATE FREQUENCY	**45.75MHz**
-INTER-CARRIER FREQUENCY	

	4.5MHz (BTSC)
CHROMA IF FREQUENCY	42.17MHz
CHANNELS RECEIVED	USA 216 Channel (AIR 2-83 Channel) CAT V (STD IRC HRC) 1-134 Channel
TUNING MODE	PLL SYSTEM
AV IN / OUT	1 A V 1 in, 1 A V 2 in, 1 S-Video in Y Cb Cr in ,Y Pb Pr in 1 AV out
AV IN/OUT SPECIFICATION	Y/C in -Y： 1.0 ± 0.2 VP-P 75Ω C: 0.7 VP-P 75Ω
	Video in ----1.0 ± 0.2 VP-P 75Ω
	Audio in ----Approx, 500mV
	Video out----1.0 ± 0.2 VP-P 75Ω
	Audio out ----Approx, 400mV
	RGB IN : ≤ 0.7 VP-P
ANTENNA INPUT IMPEDANCE	75 OHM
OSD LANGUAGE	ENGLISH / SPAINISH / GERMAN / FRENCH / PORTUGUES
AUDIO OUTPUT POWER	6Wx2 (1KHz, 0.5Vrms, 10%THD)
LED INDICATORS	Continue shine Power on Flash standby
HAND SET POWER SUPLY	Battery 1.5V （AAA）x 2

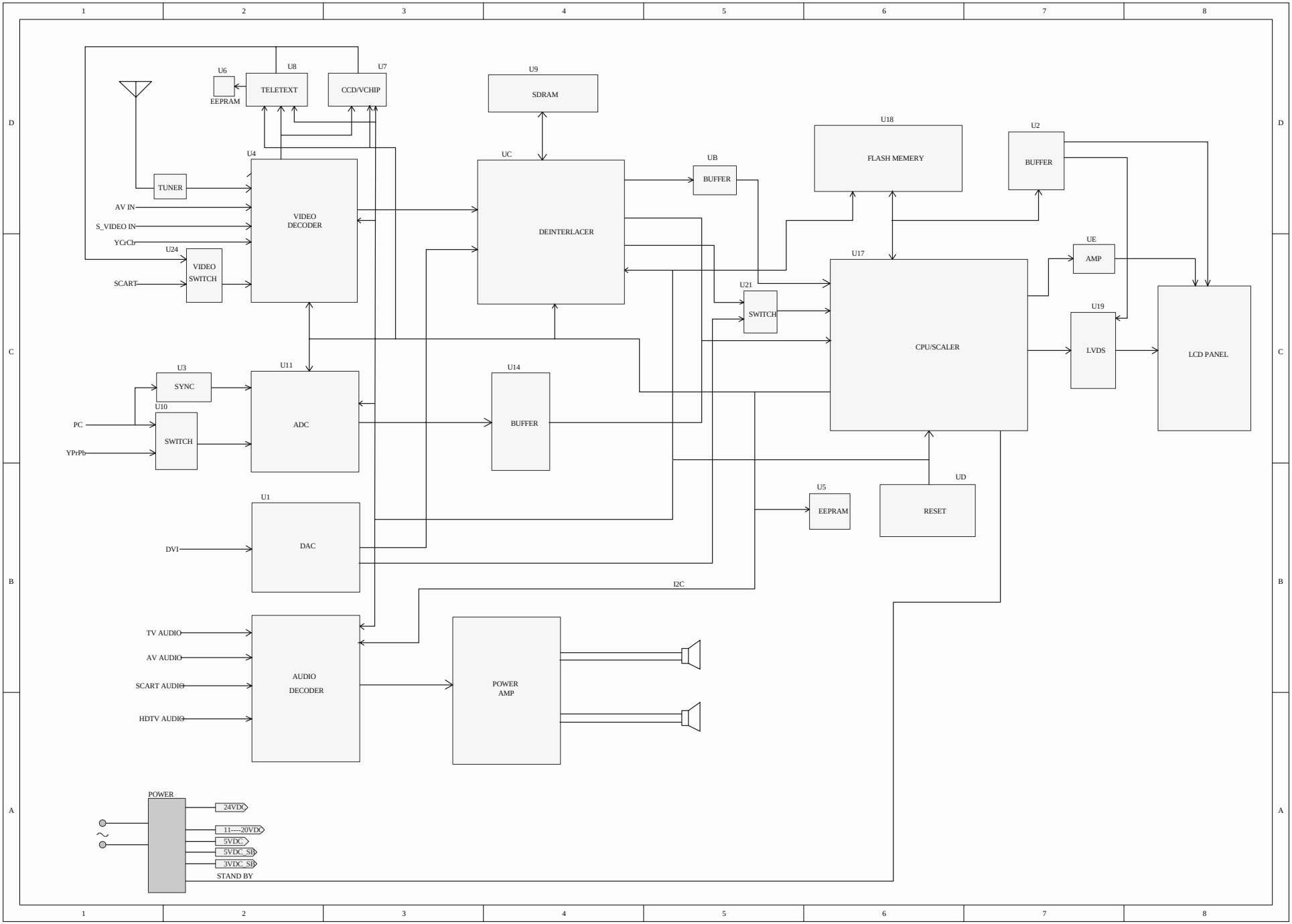
PART 2: PC RESOLUTION

ANALOG RGB IN		**0.7 VP-P**	
RESOLUTION	**V. Feq. (Hz)**	**h. Feq. (Hz)**	**GRAPHIC MODE**
640X480	**59.940**	**31.469**	**VGA**
800X600	**60.317**	**37.879**	**VGA**
1024X768	**60.004**	**48.363**	**VGA**
1280X720	**59.870**	**47.776**	**VGA**

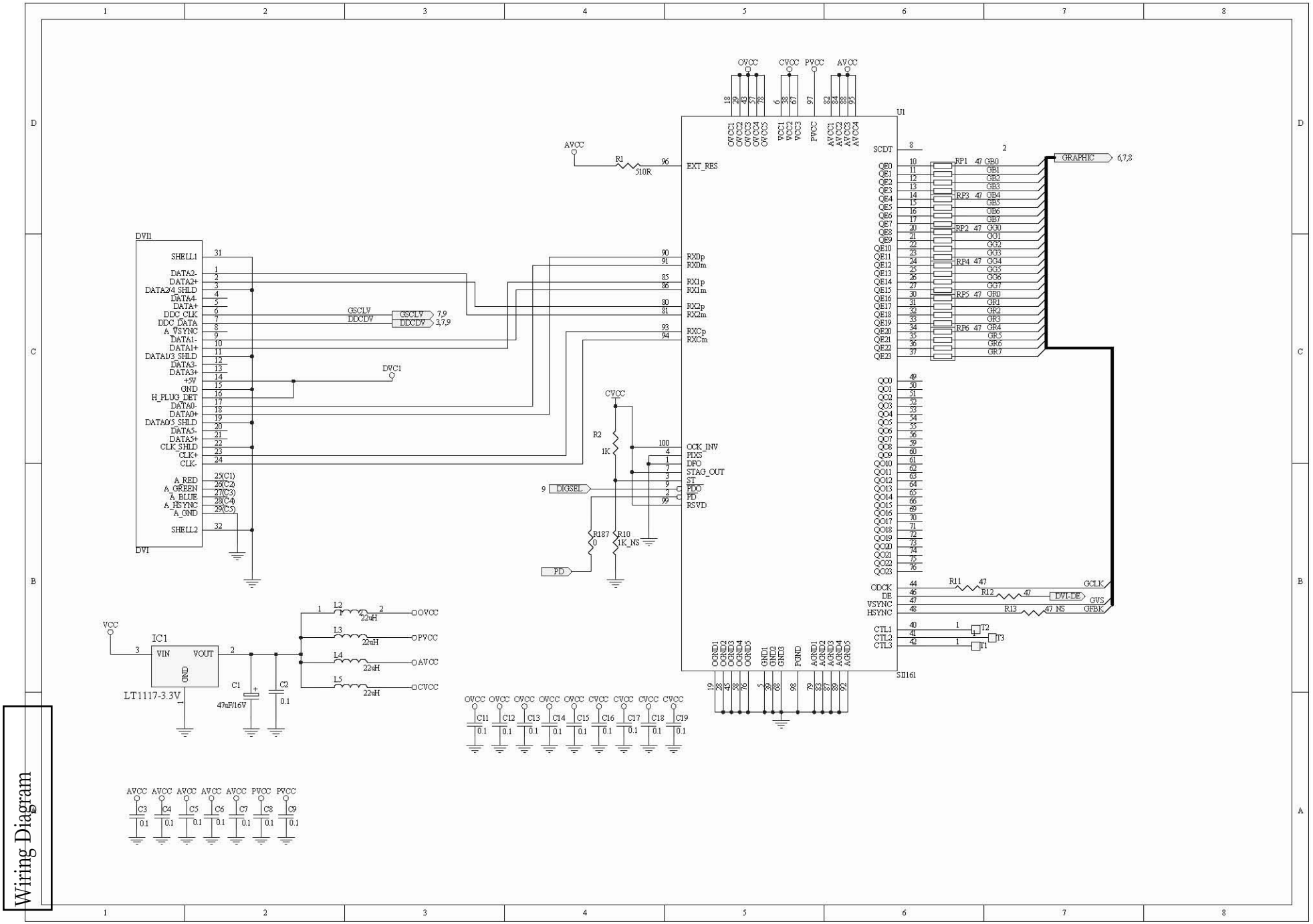
PART 3: PANEL

Brand & Model	**CHIMEI/V270W1-L03**
Resolution	**1280X720**
Displayable Colour	**16.7MHz**
Surface	**Hard Coating + Anti-Radiation**
Viewing Angle (H/V)	**170° (Hor) / 170° (Ver)**
Display Response Time	**25ms**
Contrast Ratio	**1:600**
Brightness	**550nit**
Aspect	**16;9**
Lamp Life	**50,000Hrs**
Bad Pixel Quality (Bright/Dark/Total)	**2 /6 / 8**

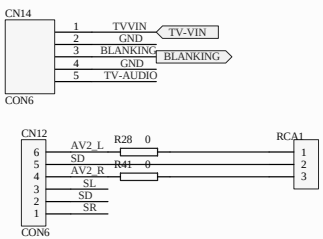
Block Diagram



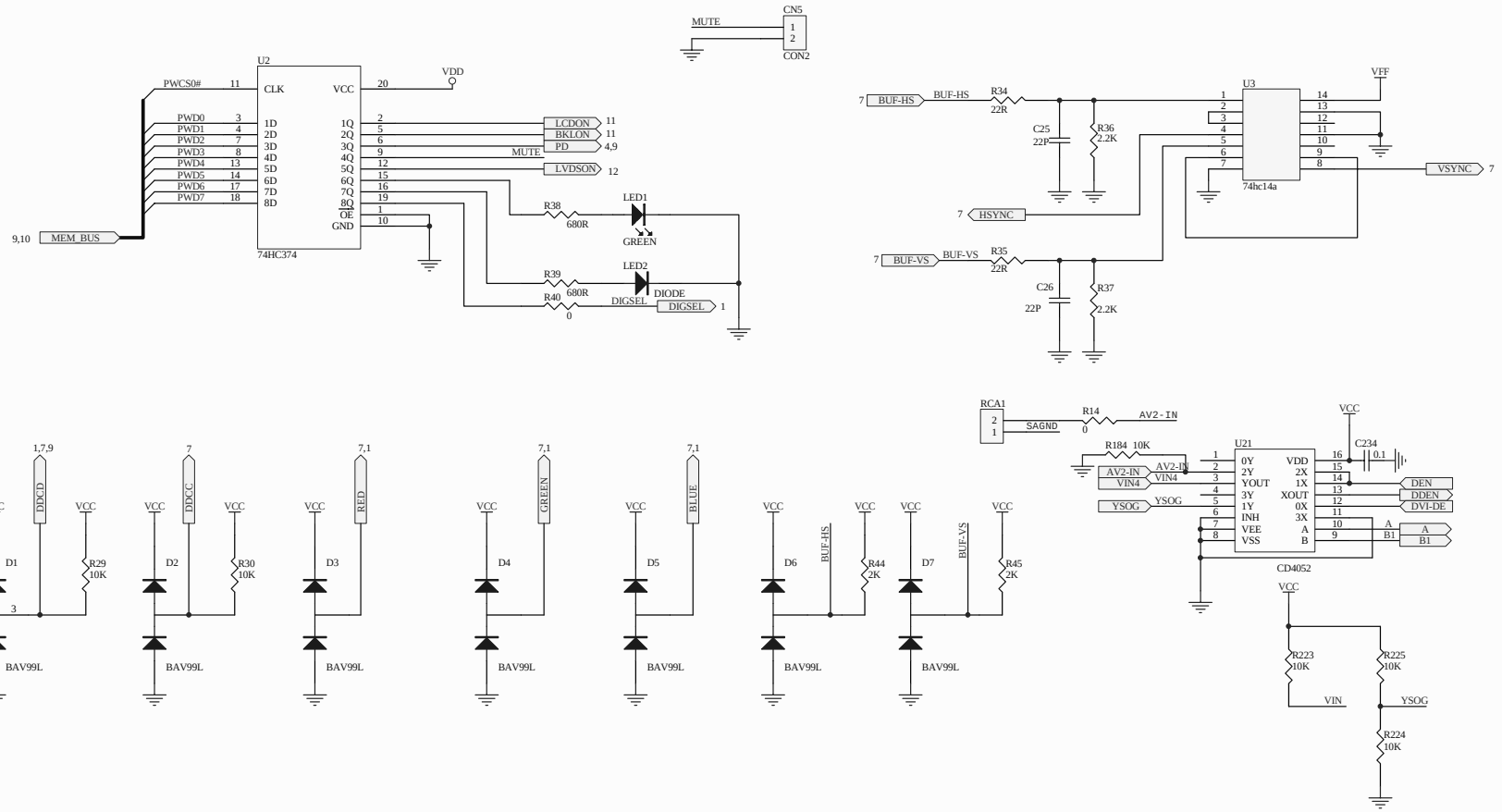
Circuit diagram

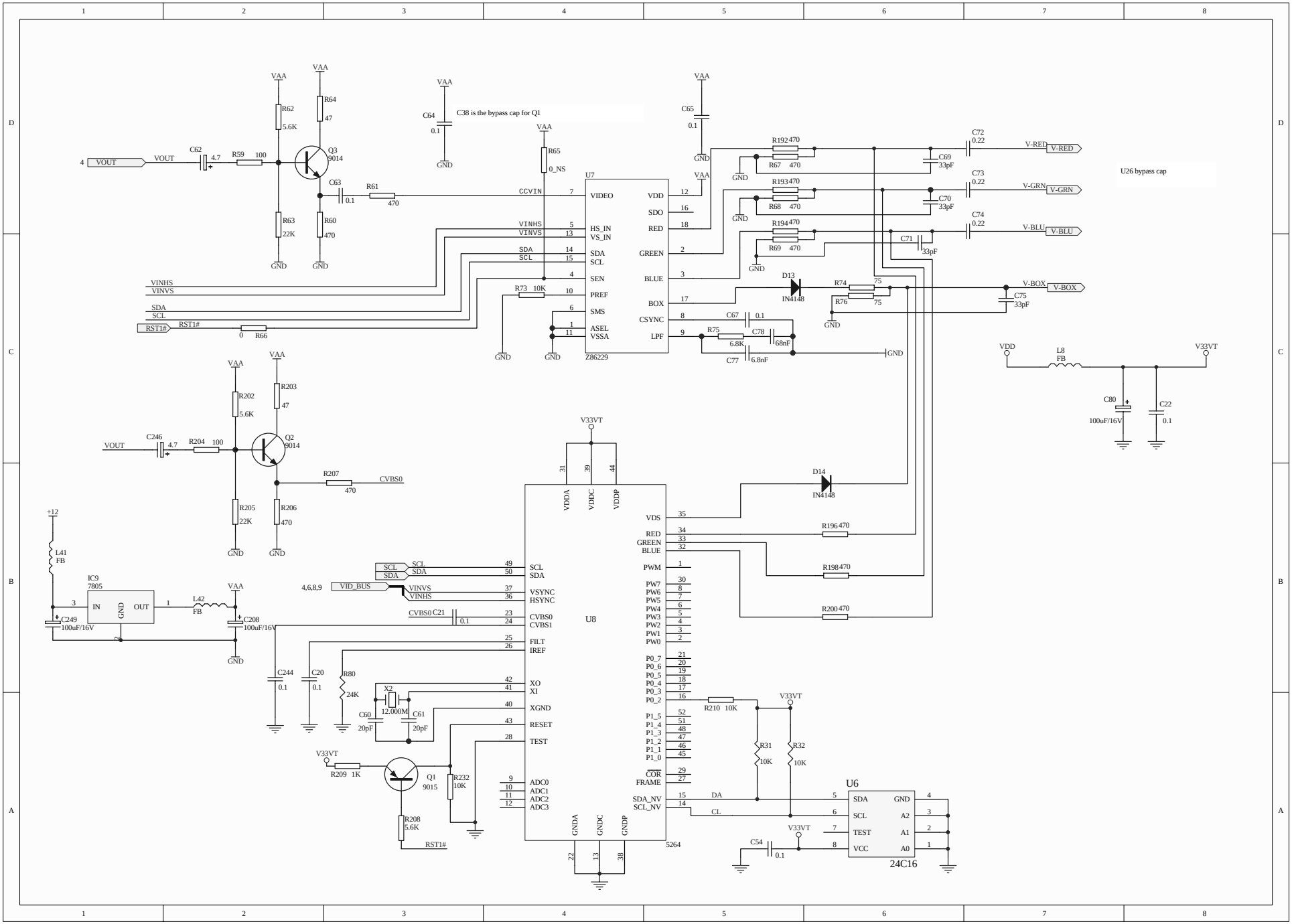


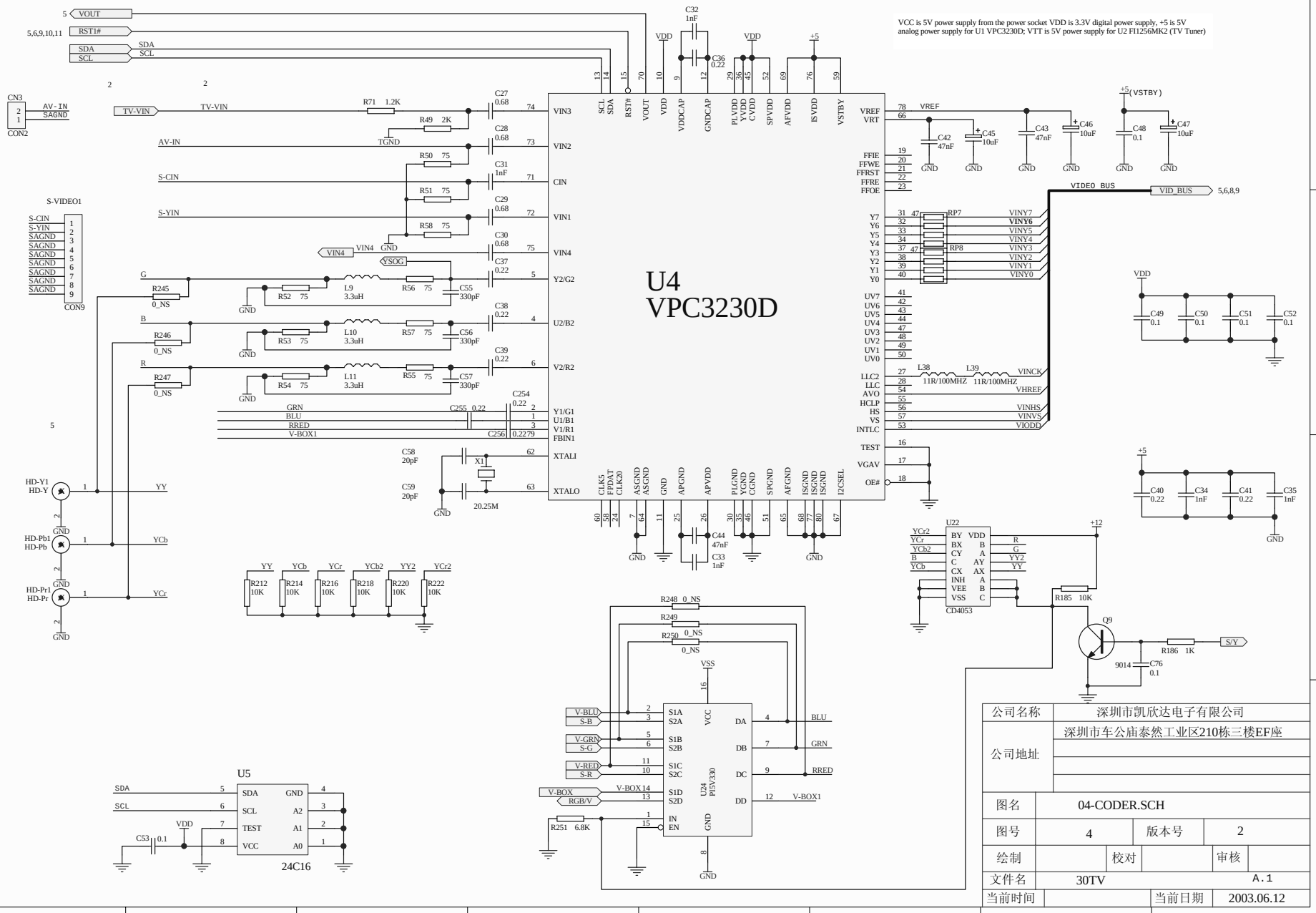
Wiring Diagram

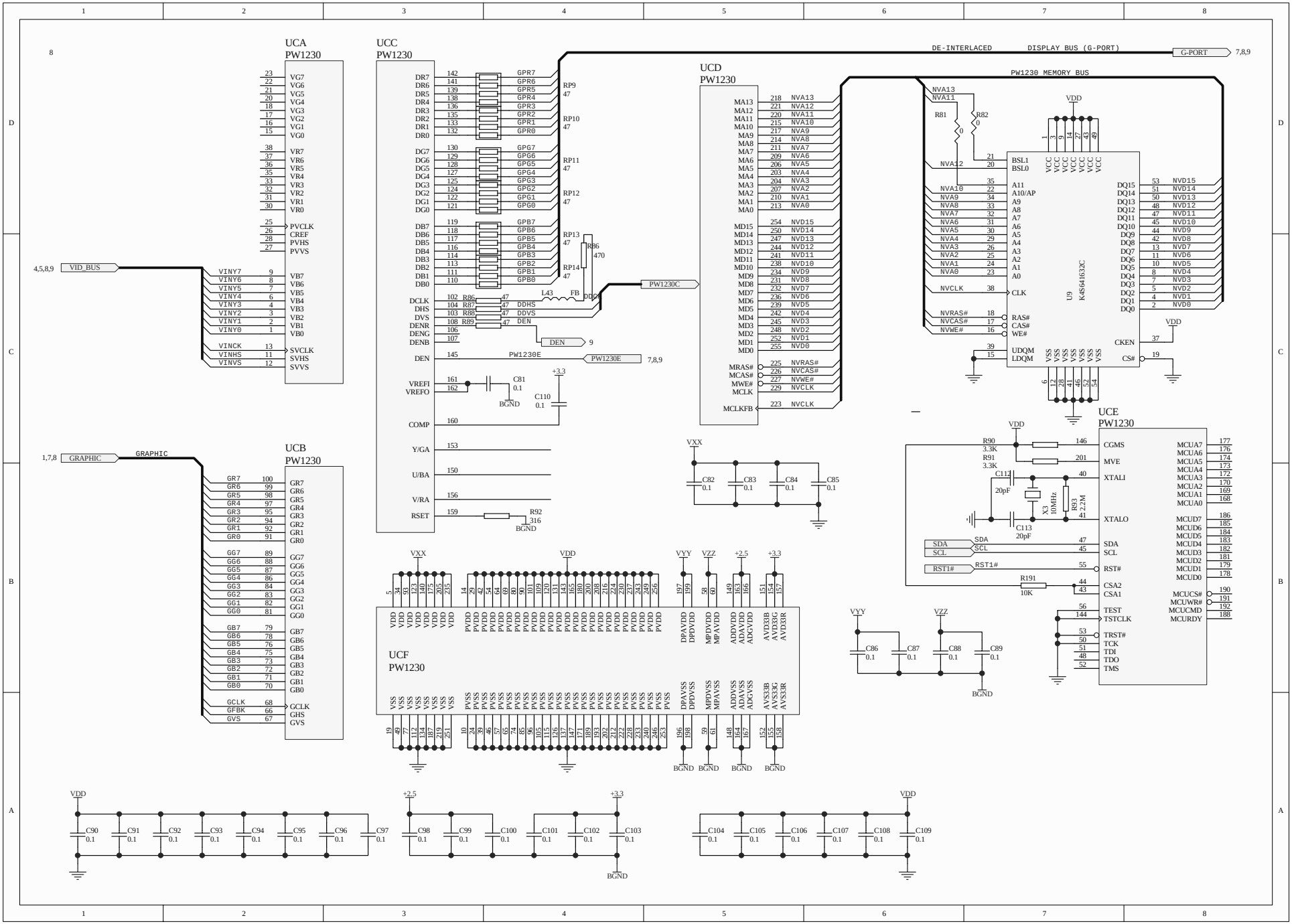

CN14
1 TVVIN
2 GND
3 BLANKING
4 GND
5 TV-AUDIO
TV-VIN
BLANKING
CON6
CN12
6
5
4
3
2
1
AV2_L
SD
AV2_R
SL
SD
SR
R28 0
R41 0
RCA1
1
2
3
CON6

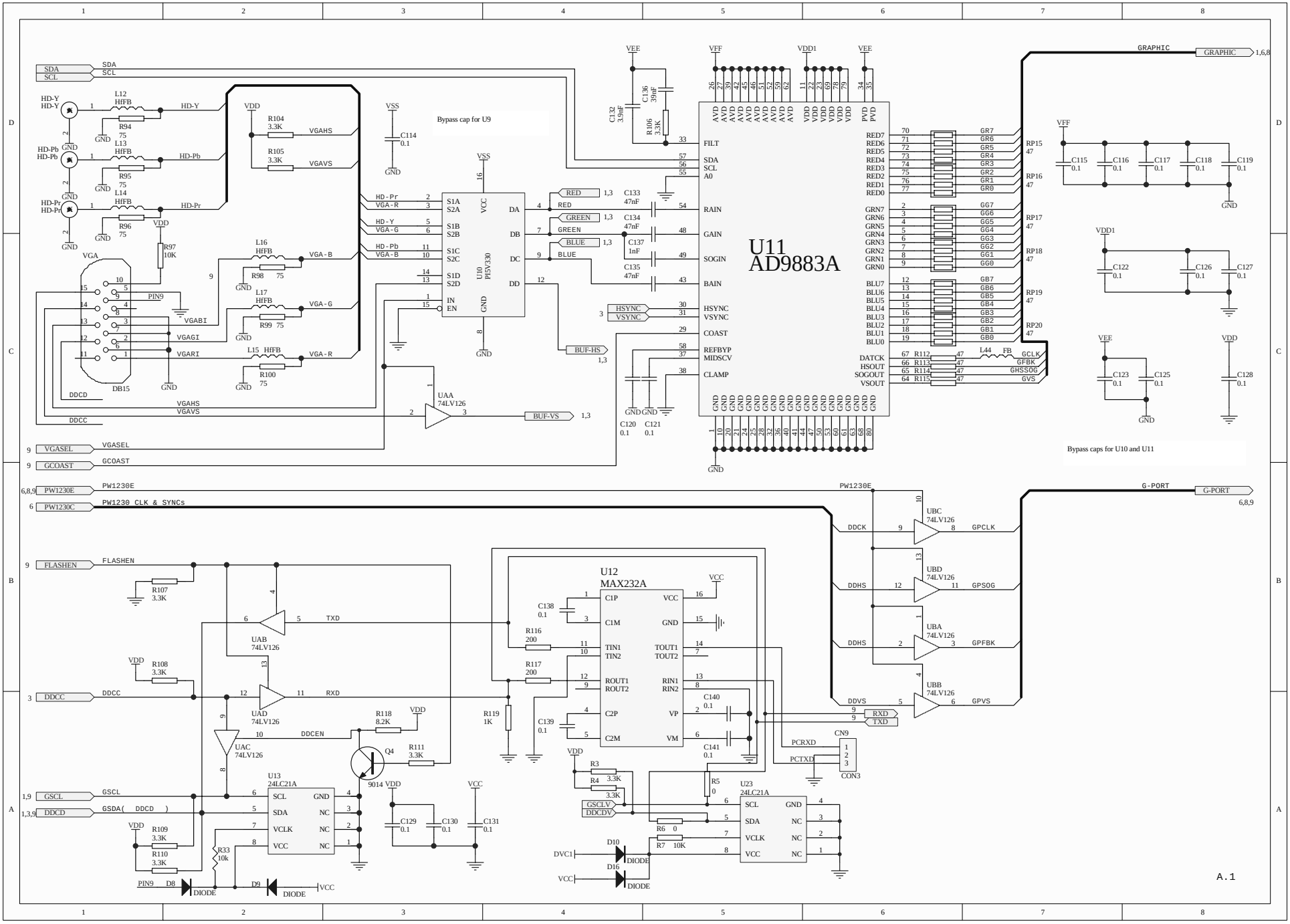
CON5 is for LCD control (J24's) supplement,

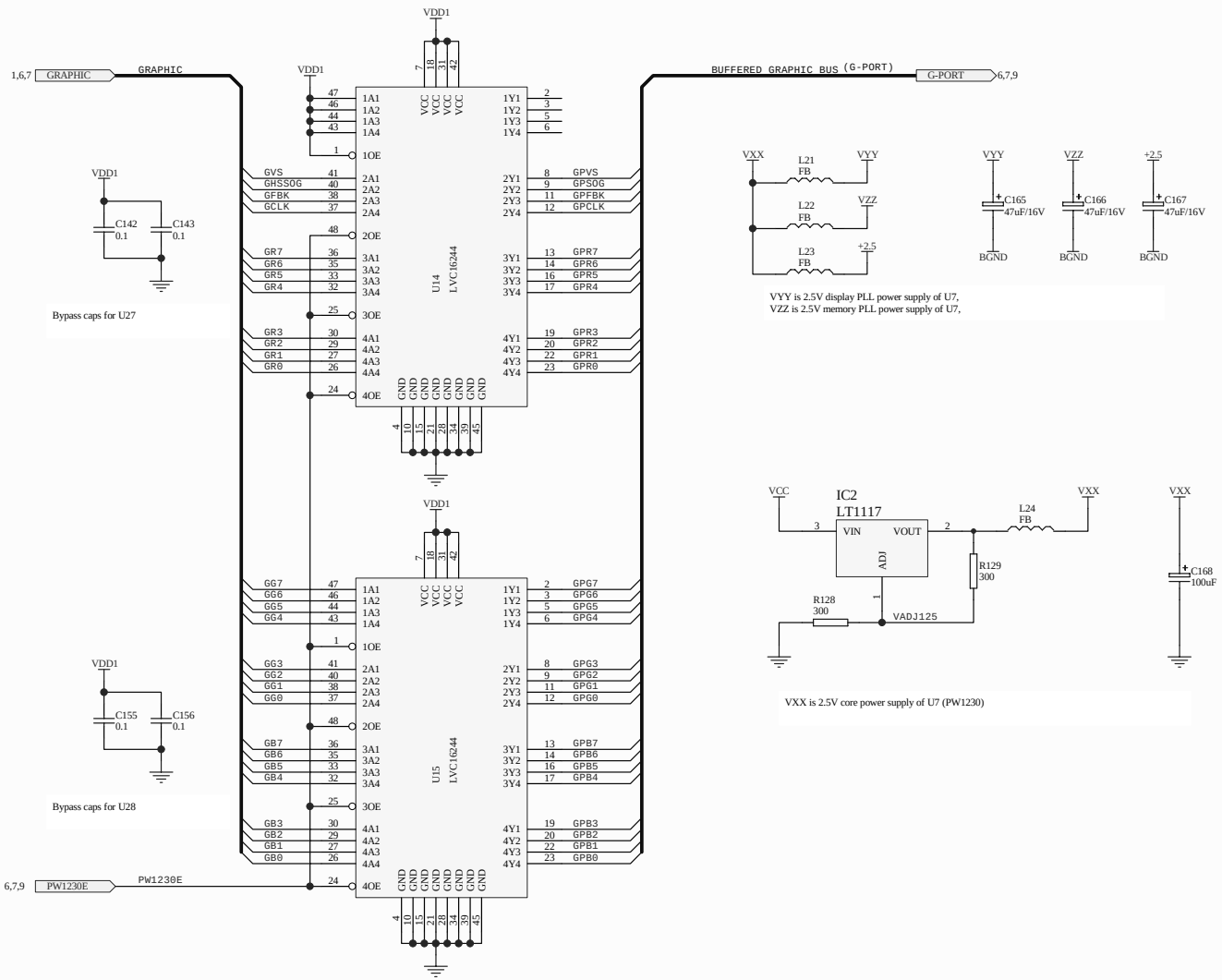



C38 is the bypass cap for Q1
U26 bypass cap
U7
Z86229
U8
5264
U6
24C16
IC9
7805
Q1
9015
Q2
9014
Q3
9014
IN4148
IN4148
X2
12.000M
VID_BUS
V-RED
V-GRN
V-BLU
V-BOX
RST1#
VOUT
VINHS
VINVS
SDA
SCL
CVBS0
V33VT
+12
VAA
GND

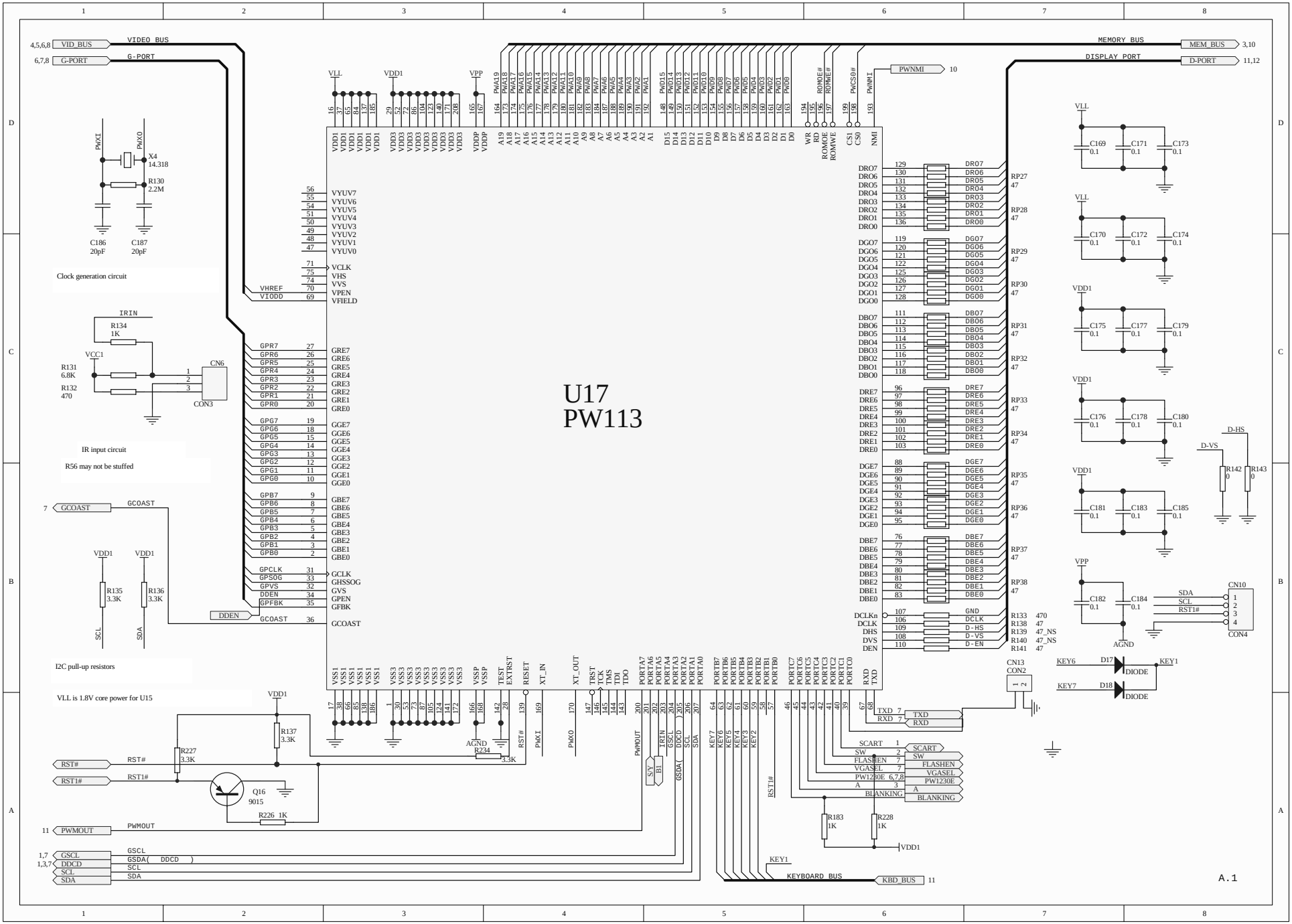

VCC is 5V power supply from the power socket VDD is 3.3V digital power supply, +5 is 5V analog power supply for U1 VPC3230D; VTT is 5V power supply for U2 FI1256MK2 (TV Tuner)
U4
VPC3230D
U5
24C16
CD4053
VIDEO BUS
公司名称 深圳市凯欣达电子有限公司
公司地址 深圳市车公庙泰然工业区210栋三楼EF座
图名 04-CODER.SCH
图号 4 版本号 2
绘制 校对 审核
文件名 30TV A.1
当前时间 当前日期 2003.06.12

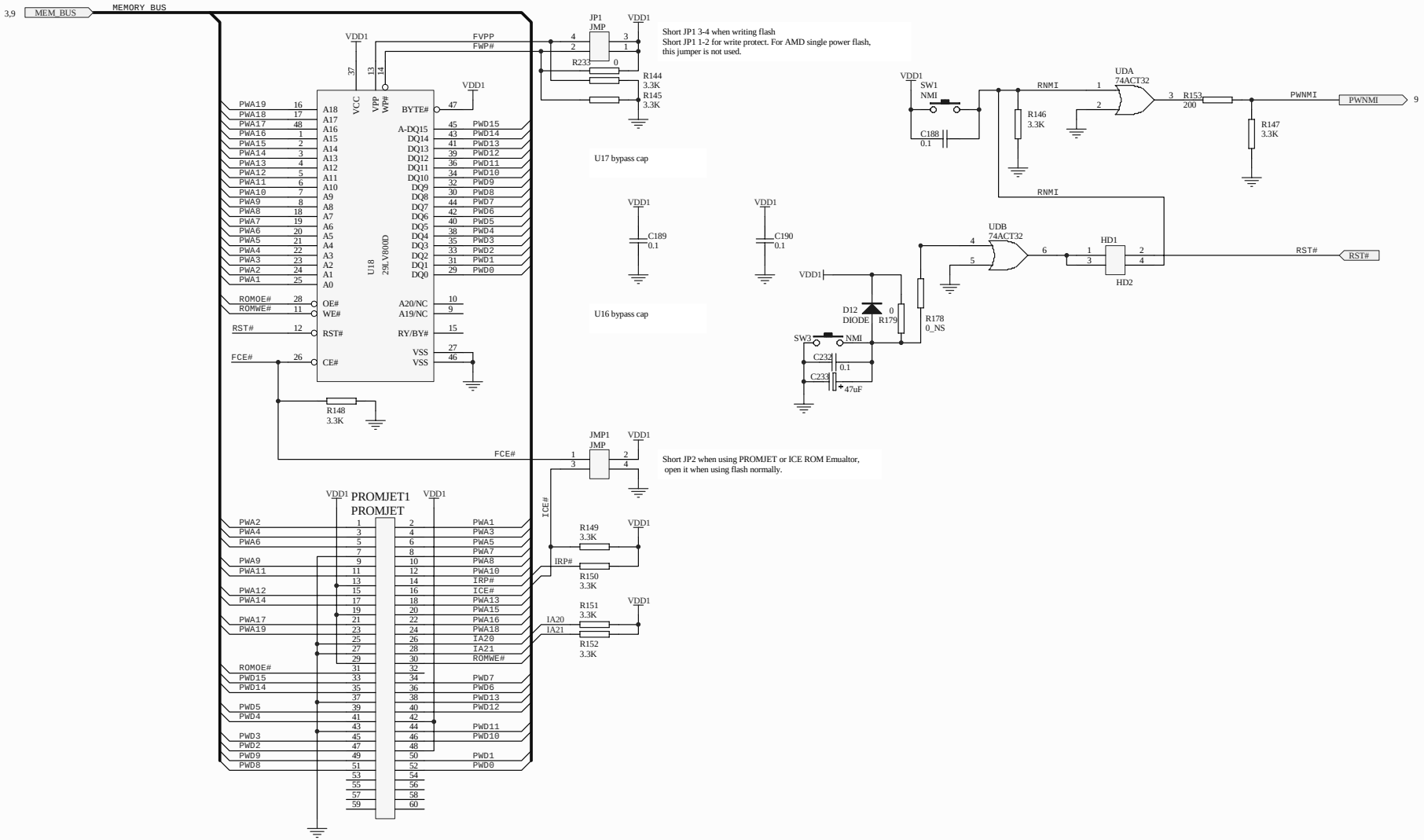

UCA
PW1230
UCC
PW1230
UCD
PW1230
UCB
PW1230
UCE
PW1230
UCF
PW1230
DE-INTERLACED DISPLAY BUS (G-PORT)
G-PORT
PW1230 MEMORY BUS
VID_BUS
GRAPHIC
PW1230C
PW1230E
DEN
DDHS
DDVS
K4S641632C
VDD
VXX
VYY
VZZ
BGND

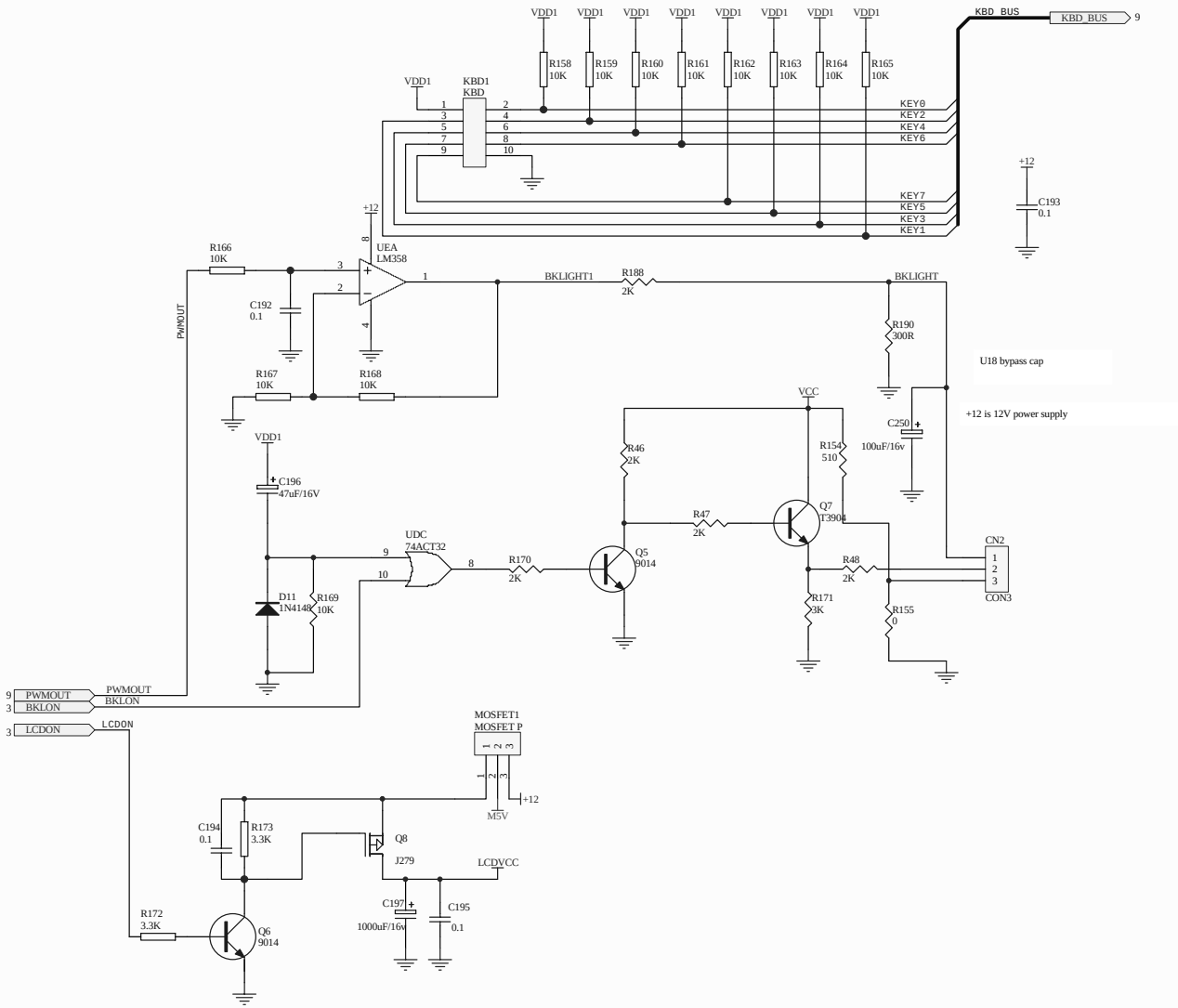

U11
AD9883A
U10
PI5V330
U12
MAX232A
U13
24LC21A
U23
24LC21A
Bypass cap for U9
Bypass caps for U10 and U11
SDA
SCL
HD-Y
HD-Pb
HD-Pr
VGA
DB15
VGABI
VGAGI
VGARI
PIN9
DDCD
DDCC
VGAHS
VGAVS
VGASEL
GCOAST
BUF-HS
BUF-VS
UAA
74LV126
UAB
74LV126
UAC
74LV126
UAD
74LV126
UBA
74LV126
UBB
74LV126
UBC
74LV126
UBD
74LV126
GRAPHIC
G-PORT
PW1230E
PW1230 CLK & SYNCs
FLASHEN
GSCL
GSDA(DDCD)
TXD
RXD
DDCEN
PCRXD
PCTXD
CON3
CN9
GSCLV
DDCDV
DVC1
DIODE
Q4
9014
A.1

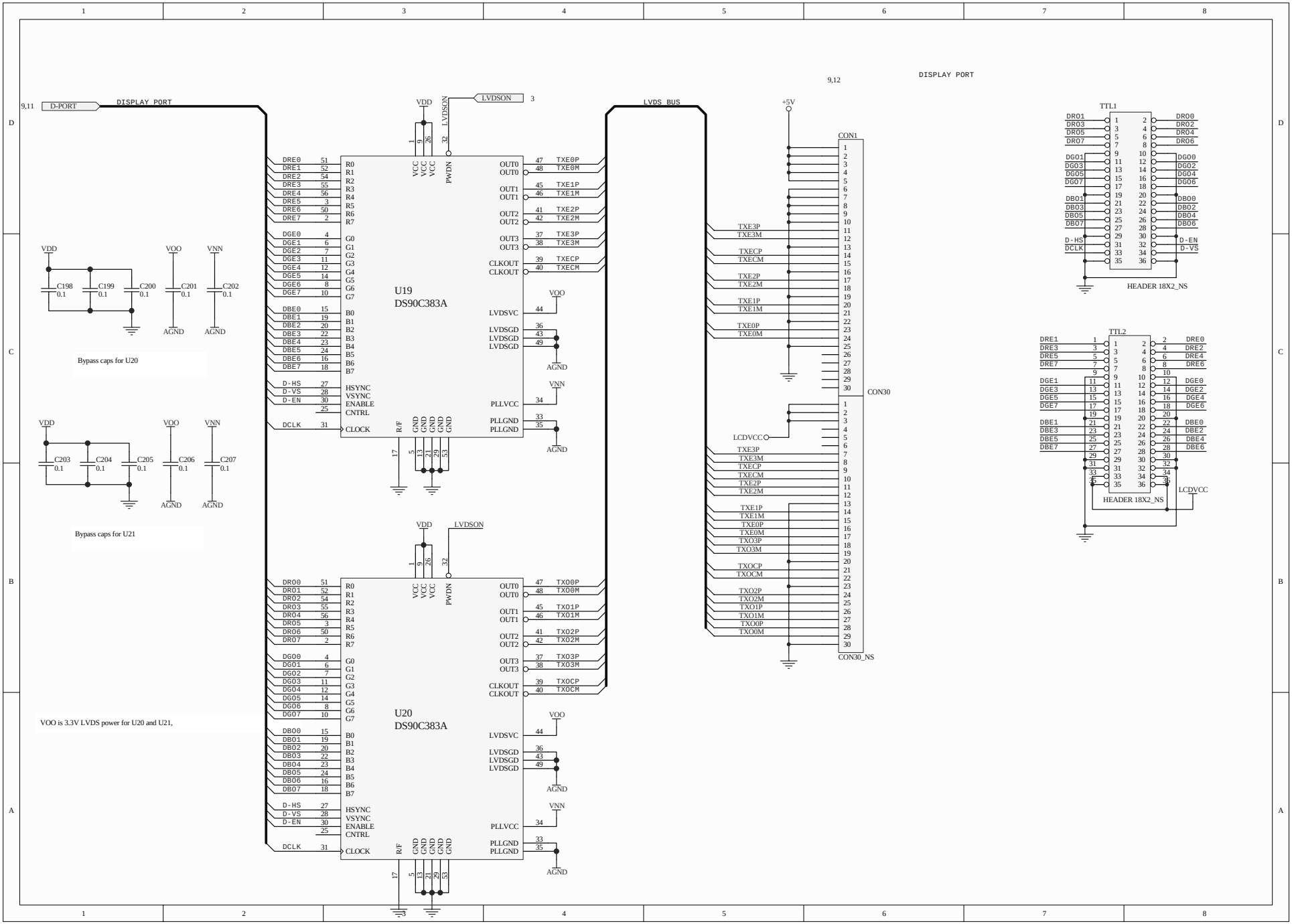

VDD1
1,6,7 GRAPHIC
GRAPHIC
U14 LVC16244
U15 LVC16244
1OE
2OE
3OE
4OE
VCC
GND
BUFFERED GRAPHIC BUS (G-PORT)
G-PORT 6,7,9
PW1230E
6,7,9 PW1230E
C142 0.1
C143 0.1
C155 0.1
C156 0.1
Bypass caps for U27
Bypass caps for U28
VXX
VYY
VZZ
+2.5
L21 FB
L22 FB
L23 FB
C165 47uF/16V
C166 47uF/16V
C167 47uF/16V
BGND
VYY is 2.5V display PLL power supply of U7,
VZZ is 2.5V memory PLL power supply of U7,
VCC
IC2
LT1117
VIN
VOUT
ADJ
L24 FB
R129 300
R128 300
VADJ125
C168 100uF
VXX is 2.5V core power supply of U7 (PW1230)

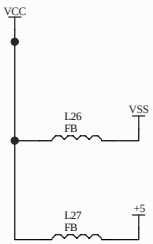
A.1

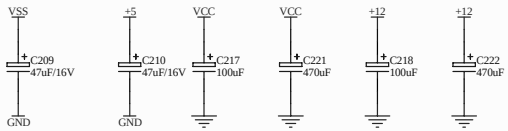

U17
PW113
VIDEO BUS
G-PORT
MEMORY BUS
DISPLAY PORT
MEM_BUS
D-PORT
PWNMI
Clock generation circuit
IR input circuit
R56 may not be stuffed
I2C pull-up resistors
VLL is 1.8V core power for U15
KEYBOARD_BUS
A.1

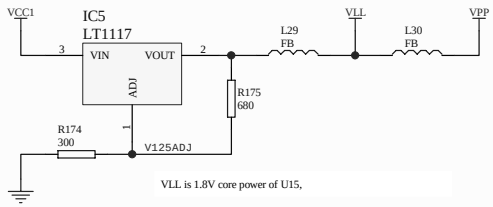

3,9
MEM_BUS
MEMORY BUS
VDD1
FVPP
FWP#
JP1
JMP
Short JP1 3-4 when writing flash
Short JP1 1-2 for write protect. For AMD single power flash, this jumper is not used.
R233
R144 3.3K
R145 3.3K
U18
29L V800D
PWA19
PWA18
PWA17
PWA16
PWA15
PWA14
PWA13
PWA12
PWA11
PWA10
PWA9
PWA8
PWA7
PWA6
PWA5
PWA4
PWA3
PWA2
PWA1
ROMOE#
ROMWE#
RST#
FCE#
BYTE#
A-DQ15
PWD15
PWD14
PWD13
PWD12
PWD11
PWD10
PWD9
PWD8
PWD7
PWD6
PWD5
PWD4
PWD3
PWD2
PWD1
PWD0
A20/NC
A19/NC
RY/BY#
R148 3.3K
U17 bypass cap
U16 bypass cap
C189 0.1
C190 0.1
SW1
NMI
C188 0.1
R146 3.3K
RNMI
UDA
74ACT32
R153 200
PWNMI
R147 3.3K
UDB
74ACT32
HD1
HD2
RST#
D12
DIODE
R179 0
R178 0_NS
SW3
C232 0.1
C233 47uF
JMP1
Short JP2 when using PROMJET or ICE ROM Emualtor, open it when using flash normally.
ICE#
IRP#
IA20
IA21
R149 3.3K
R150 3.3K
R151 3.3K
R152 3.3K
PROMJET1
PROMJET


VDD1
KBD_BUS
R158 10K
R159 10K
R160 10K
R161 10K
R162 10K
R163 10K
R164 10K
R165 10K
KBD1
KBD
KEY0
KEY2
KEY4
KEY6
KEY7
KEY5
KEY3
KEY1
+12
C193 0.1
R166 10K
UEA LM358
C192 0.1
PWMOUT
R167 10K
R168 10K
BKLIGHT1
R188 2K
BKLIGHT
R190 300R
U18 bypass cap
+12 is 12V power supply
VCC
C250 100uF/16v
R154 510
R46 2K
R47 2K
Q7 T3904
C196 47uF/16V
UDC 74ACT32
R170 2K
Q5 9014
D11 1N4148
R169 10K
R48 2K
R171 3K
R155 0
CN2
CON3
PWMOUT
BKLON
LCDON
MOSFET1
MOSFET P
M5V
C194 0.1
R173 3.3K
Q8
J279
LCDVCC
R172 3.3K
Q6 9014
C197 1000uF/16v
C195 0.1

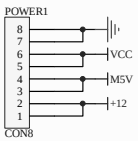

DISPLAY PORT
9,11
D-PORT
DISPLAY PORT
9,12
DISPLAY PORT
LVDSON
3
LVDS BUS
U19
DS90C383A
U20
DS90C383A
Bypass caps for U20
Bypass caps for U21
VOO is 3.3V LVDS power for U20 and U21,
CON1
CON30
CON30_NS
TTL1
TTL2
HEADER 18X2_NS
HEADER 18X2_NS
LCDVCC
+5V
VDD
VOO
VNN
AGND

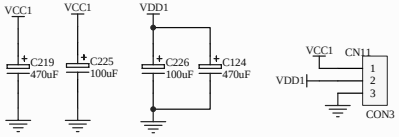


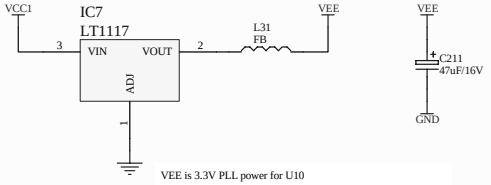




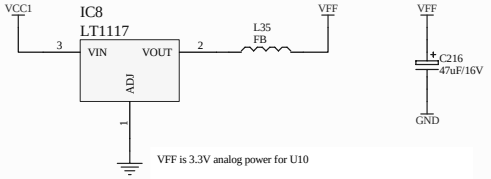
VLL is 1.8V core power of U15,





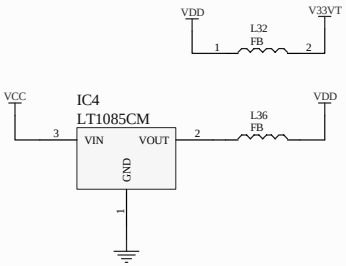


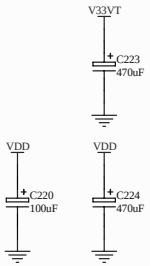
VEE is 3.3V PLL power for U10

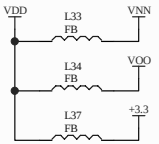


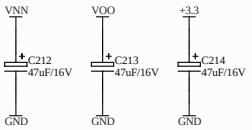
VFF is 3.3V analog power for U10

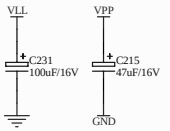
J28' and J28" are supplementary power sockets



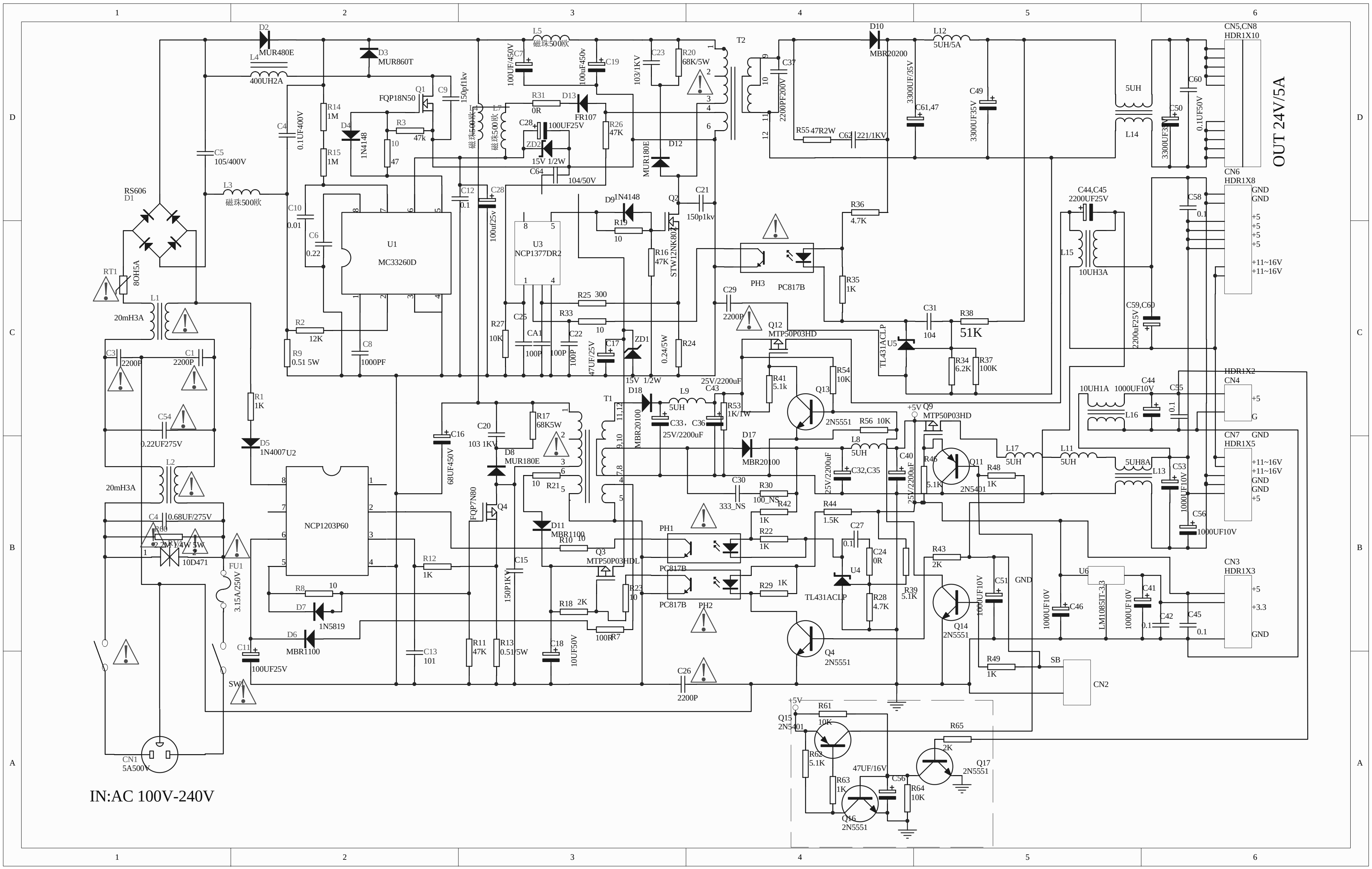


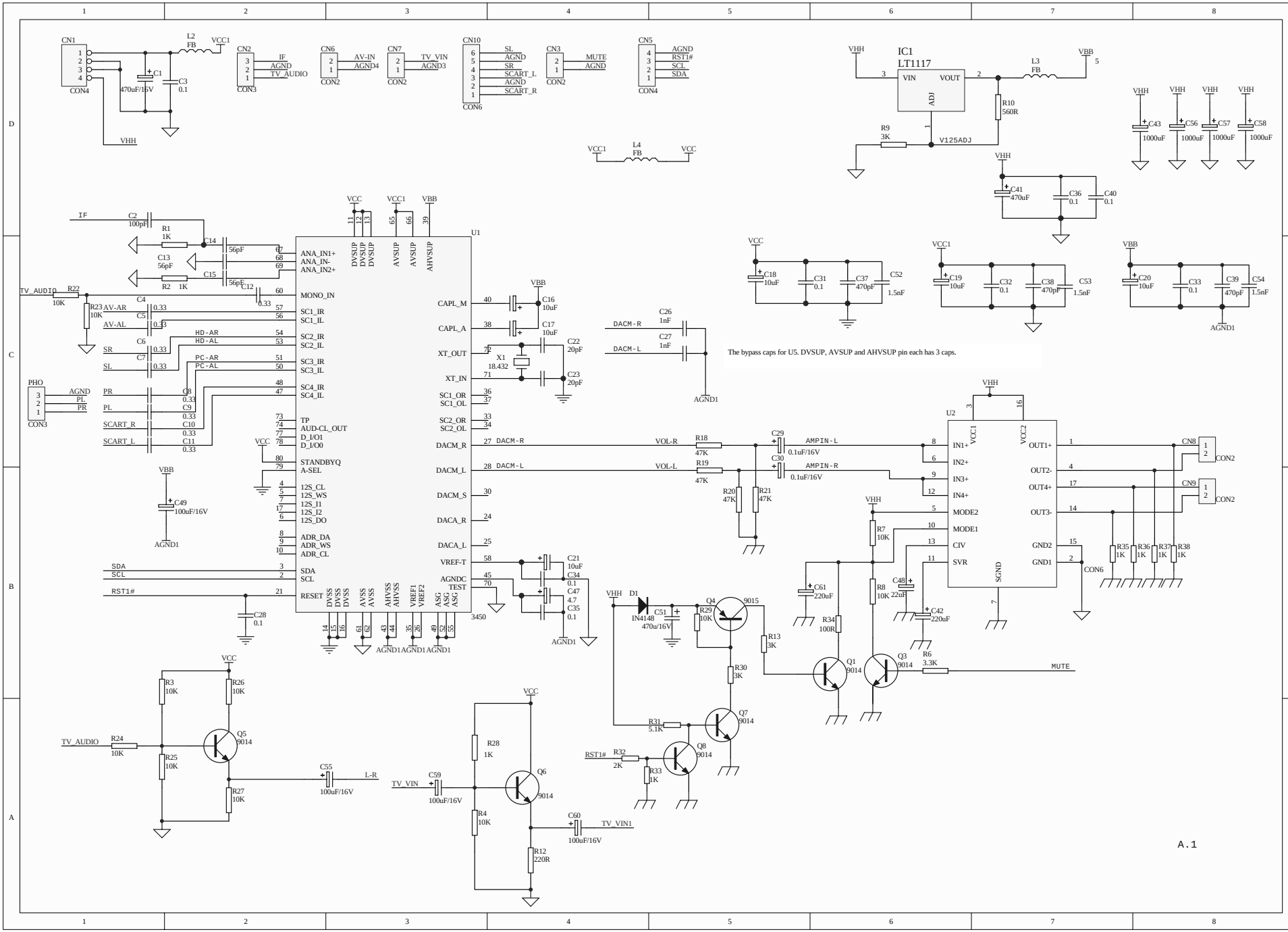


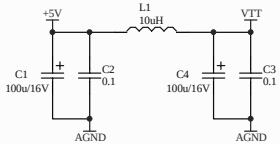


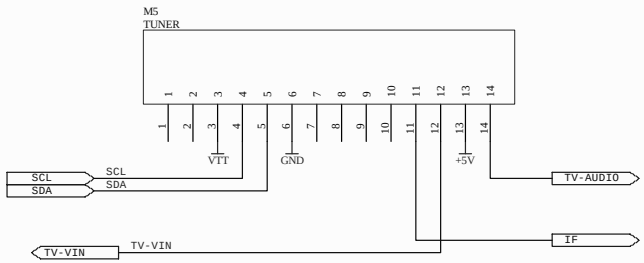


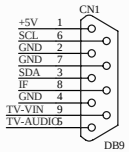
CK3 is the decoupling cap for VLL,


IN:AC 100V-240V
OUT 24V/5A
CN1
5A500V
SW
FU1
3.15A/250V
RV1
10D471
RT1
8OH5A
L1
20mH3A
L2
20mH3A
C1
2200P
C3
2200P
C54
0.22UF275V
C4
0.68UF/275V
RS606
D1
C5
105/400V
L3
磁珠500欧
L4
400UH2A
D2
MUR480E
D3
MUR860T
Q1
FQP18N50
C9
150pf1kv
D4
1N4148
R14
1M
R15
1M
R3
47k
C4
0.1UF400V
U1
MC33260D
C10
0.01
C6
0.22
R2
12K
R9
0.51 5W
C8
1000PF
C12
0.1
C28
100uf25v
L5
磁珠500欧
C7
100UF/450V
C19
100uF450v
C23
103/1KV
R20
68K/5W
T2
R31
0R
D13
FR107
R26
47K
ZD2
15V 1/2W
C64
104/50V
D12
MUR180E
U3
NCP1377DR2
D9
1N4148
R19
10
Q2
STW12NK80Z
C21
150p1kv
R16
47K
R25
300
R33
10
R27
10K
C25
CA1
100P
C22
100P
C17
47UF/25V
ZD1
15V 1/2W
R24
0.24/5W
C29
2200P
C37
2200PF200V
D10
MBR20200
L12
5UH/5A
C61,47
3300UF/35V
C49
3300UF35V
R55
47R2W
C62
221/1KV
5UH
L14
C50
3300UF35V
C60
0.1UF50V
CN5,CN8
HDR1X10
CN6
HDR1X8
GND
GND
+5
+5
+5
+5
+11~16V
+11~16V
C58
0.1
C44,C45
2200UF25V
L15
10UH3A
R36
4.7K
PH3
PC817B
R35
1K
C31
104
R38
51K
U5
TL431ACLP
R34
6.2K
R37
100K
C59,C60
2200uF25V
U2
NCP1203P60
D5
1N4007
R1
1K
C16
68UF450V
C20
103 1KV
R17
68K5W
D8
MUR180E
T1
D18
MBR20100
L9
5UH
C43
C33,C36
25V/2200uF
R53
1K/1W
Q12
MTP50P03HD
R41
5.1k
R54
10K
Q13
2N5551
R56
10K
+5V
Q9
MTP50P03HD
D17
MBR20100
L8
5UH
C32,C35
25V/2200uF
C40
25V/2200uF
R46
5.1K
Q11
2N5401
R48
1K
L17
5UH
L11
5UH
5UH8A
L13
C53
1000UF10V
C56
1000UF10V
CN7
HDR1X5
10UH1A
1000UF10V
C44
C55
0.1
L16
HDR1X2
CN4
G
Q4
FQP7N80
R21
10
D11
MBR1100
R10
10
Q3
MTP50P03HDL
C30
333_NS
R30
100_NS
R42
1K
R44
1.5K
PH1
PC817B
R22
1K
C27
0.1
C24
0R
U4
TL431ACLP
R39
5.1K
R28
4.7K
R43
2K
C51
1000UF10V
GND
U6
LM1085IT-3.3
C46
1000UF10V
C41
1000UF10V
C42
0.1
C45
0.1
CN3
HDR1X3
+5
+3.3
GND
Q14
2N5551
PH2
PC817B
R29
1K
R23
10
R7
100R
R18
2K
R12
1K
R8
10
D7
1N5819
D6
MBR1100
C11
100UF25V
C13
101
R11
47K
R13
0.51/5W
C15
150P1KV
C18
10UF50V
C26
2200P
Q4
2N5551
R49
1K
SB
CN2
R61
10K
Q15
2N5401
R62
5.1K
R63
1K
Q16
2N5551
47UF/16V
C56
R64
10K
R65
2K
Q17
2N5551


CN1
CON4
L2
FB
VCC1
C1
470uF/16V
C3
0.1
VHH
CN2
CON3
IF
AGND
TV_AUDIO
CN6
CON2
AV-IN
AGND4
CN7
CON2
TV_VIN
AGND3
CN10
CON6
SL
AGND
SR
SCART_L
AGND
SCART_R
CN3
CON2
MUTE
AGND
CN5
CON4
AGND
RST1#
SCL
SDA
IC1
LT1117
VIN
VOUT
ADJ
V125ADJ
R10
560R
R9
3K
L3
FB
VBB
C43
C56
C57
C58
1000uF
C41
470uF
C36
0.1
C40
0.1
L4
FB
VCC
C18
10uF
C31
0.1
C37
470pF
C52
1.5nF
C19
10uF
C32
0.1
C38
470pF
C53
1.5nF
C20
10uF
C33
0.1
C39
470pF
C54
1.5nF
AGND1
U1
ANA_IN1+
ANA_IN-
ANA_IN2+
MONO_IN
SC1_IR
SC1_IL
SC2_IR
SC2_IL
SC3_IR
SC3_IL
SC4_IR
SC4_IL
TP
AUD-CL_OUT
D_I/O1
D_I/O0
STANDBYQ
A-SEL
12S_CL
12S_WS
12S_I1
12S_I2
12S_DO
ADR_DA
ADR_WS
ADR_CL
SDA
SCL
RESET
CAPL_M
CAPL_A
XT_OUT
XT_IN
SC1_OR
SC1_OL
SC2_OR
SC2_OL
DACM_R
DACM_L
DACM_S
DACA_R
DACA_L
VREF-T
AGNDC
TEST
DVSUP
AVSUP
AHVSUP
DVSS
AVSS
AHVSS
VREF1
VREF2
ASG
3450
IF
C2
100pF
R1
1K
C14
56pF
C13
56pF
C15
56pF
R2
1K
C12
0.33
TV_AUDIO
R22
10K
R23
10K
AV-AR
AV-AL
C4
C5
C6
C7
0.33
SR
SL
HD-AR
HD-AL
PC-AR
PC-AL
PHO
CON3
PR
PL
SCART_R
SCART_L
C8
C9
C10
C11
C16
10uF
C17
10uF
C22
20pF
C23
20pF
X1
18.432
C26
1nF
C27
1nF
DACM-R
DACM-L
The bypass caps for U5. DVSUP, AVSUP and AHVSUP pin each has 3 caps.
VOL-R
VOL-L
R18
47K
R19
47K
R20
47K
R21
47K
C29
0.1uF/16V
C30
0.1uF/16V
AMPIN-L
AMPIN-R
U2
VCC1
VCC2
SGND
IN1+
IN2+
IN3+
IN4+
MODE2
MODE1
CIV
SVR
OUT1+
OUT2-
OUT4+
OUT3-
GND2
GND1
CN8
CN9
CON2
CON6
R35
R36
R37
R38
1K
R7
10K
R8
10K
C61
220uF
C48
22uF
C42
220uF
R34
100R
C21
10uF
C34
0.1
C47
4.7
C35
0.1
C49
100uF/16V
D1
IN4148
C51
470u/16V
Q4
9015
R29
10K
R30
3K
R13
3K
Q1
9014
Q3
9014
R6
3.3K
MUTE
R31
5.1K
Q7
9014
Q8
9014
RST1#
R32
2K
R33
1K
R3
10K
R26
10K
Q5
9014
TV_AUDIO
R24
10K
R25
10K
R27
10K
C55
100uF/16V
L-R
R28
1K
Q6
9014
TV_VIN
C59
100uF/16V
R4
10K
C60
100uF/16V
TV_VIN1
R12
220R
A.1

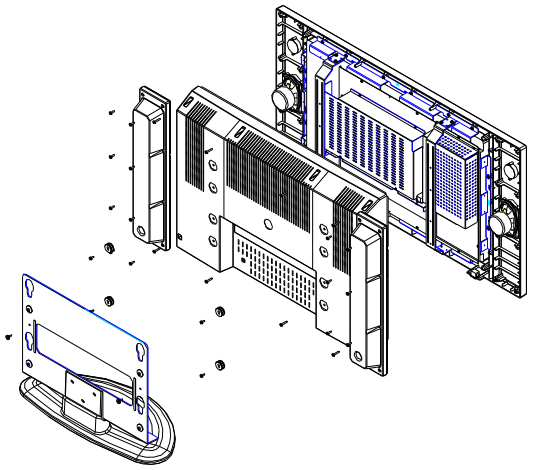

+5V
L1
10uH
VTT
C1
100u/16V
C2
0.1
C4
100u/16V
C3
0.1
AGND
AGND


M5
TUNER
1
2
3
4
5
6
7
8
9
10
11
12
13
14
VTT
GND
+5V
SCL
SDA
SCL
SDA
TV-AUDIO
IF
TV-VIN
TV-VIN

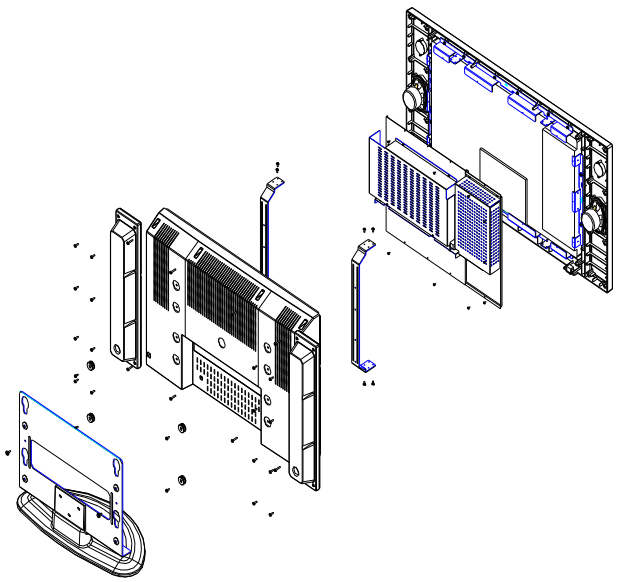

CN1
+5V 1
SCL 6
GND 2
GND 7
SDA 3
IF 8
GND 4
TV-VIN 9
TV-AUDIO 5
DB9

Disassembly

In case of trouble, etc., Necessitating disassemble, please disassemble in the order shown in the illustrations.
Reassemble in the reverse order.
1. Removal of the Back Cover

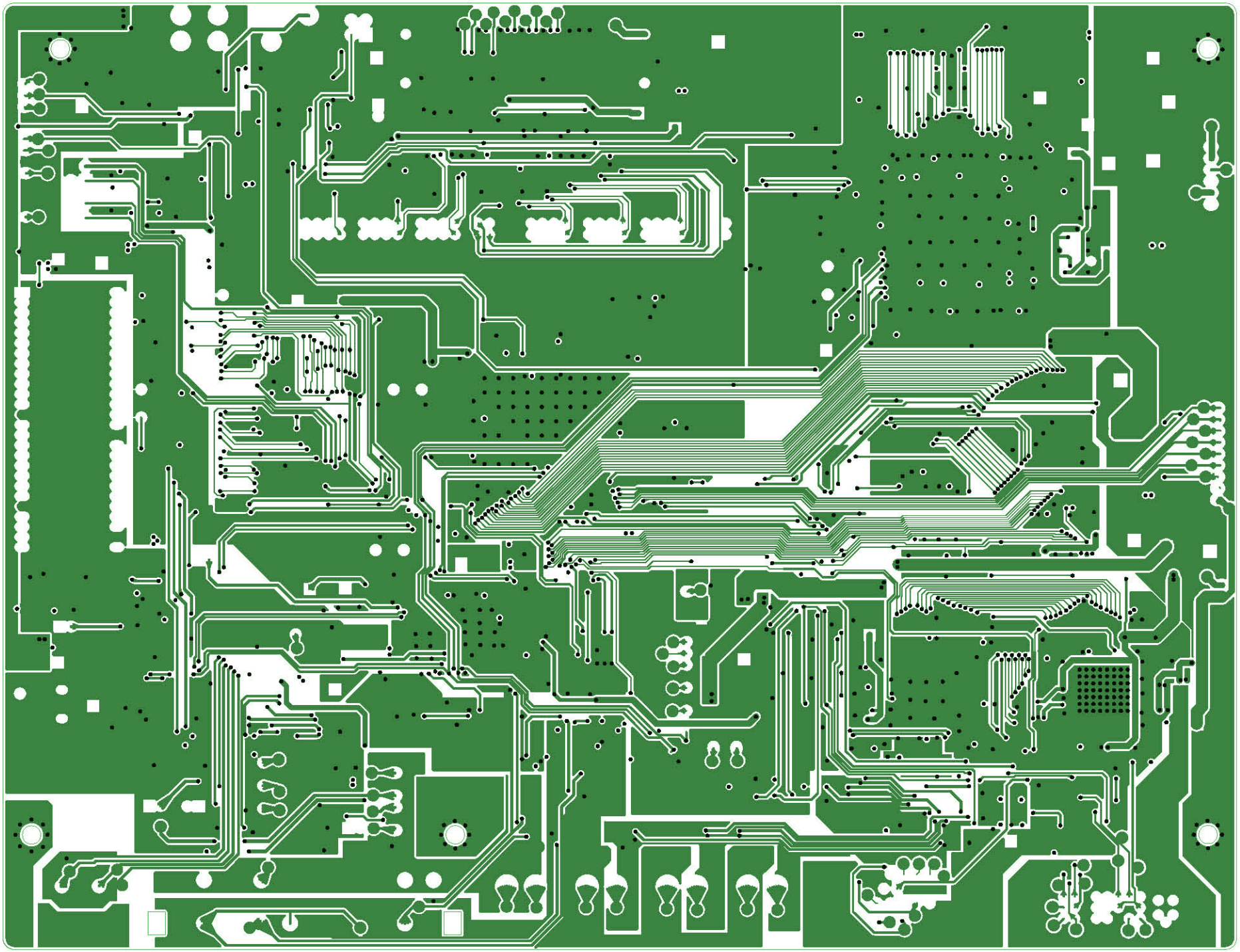


2. Removal of the MAIN PCB
   a. Remove the screws.
   b · Slide out the LCD chassis slightly; pull up the connector of AC cord from PCB; pull up the LCD PCB from LCD.
   c . Remove the Anode cap from Thepicture tube. To avaid a shock hazard, be sure to discharge
   d · Take out the LCD chassis.

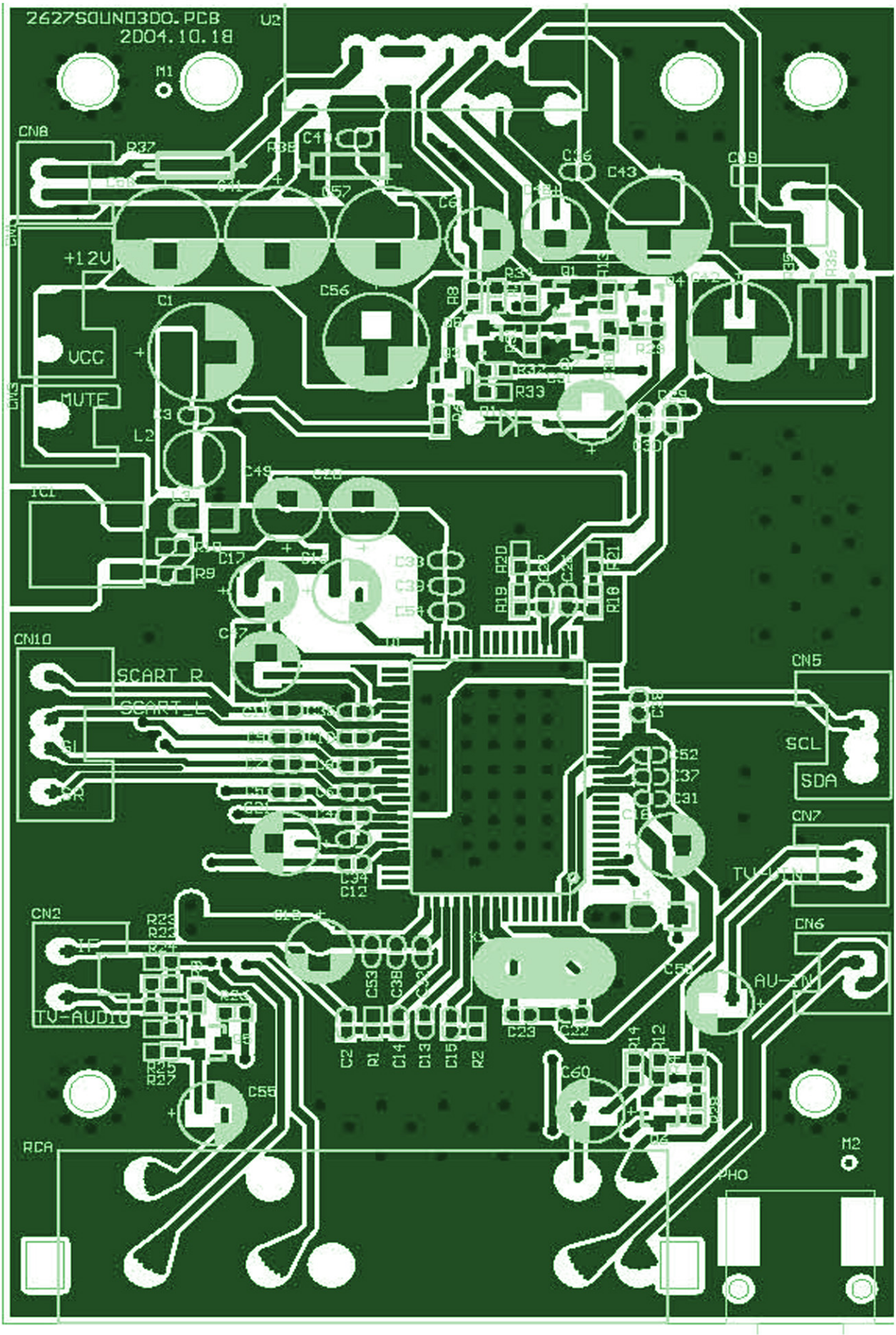


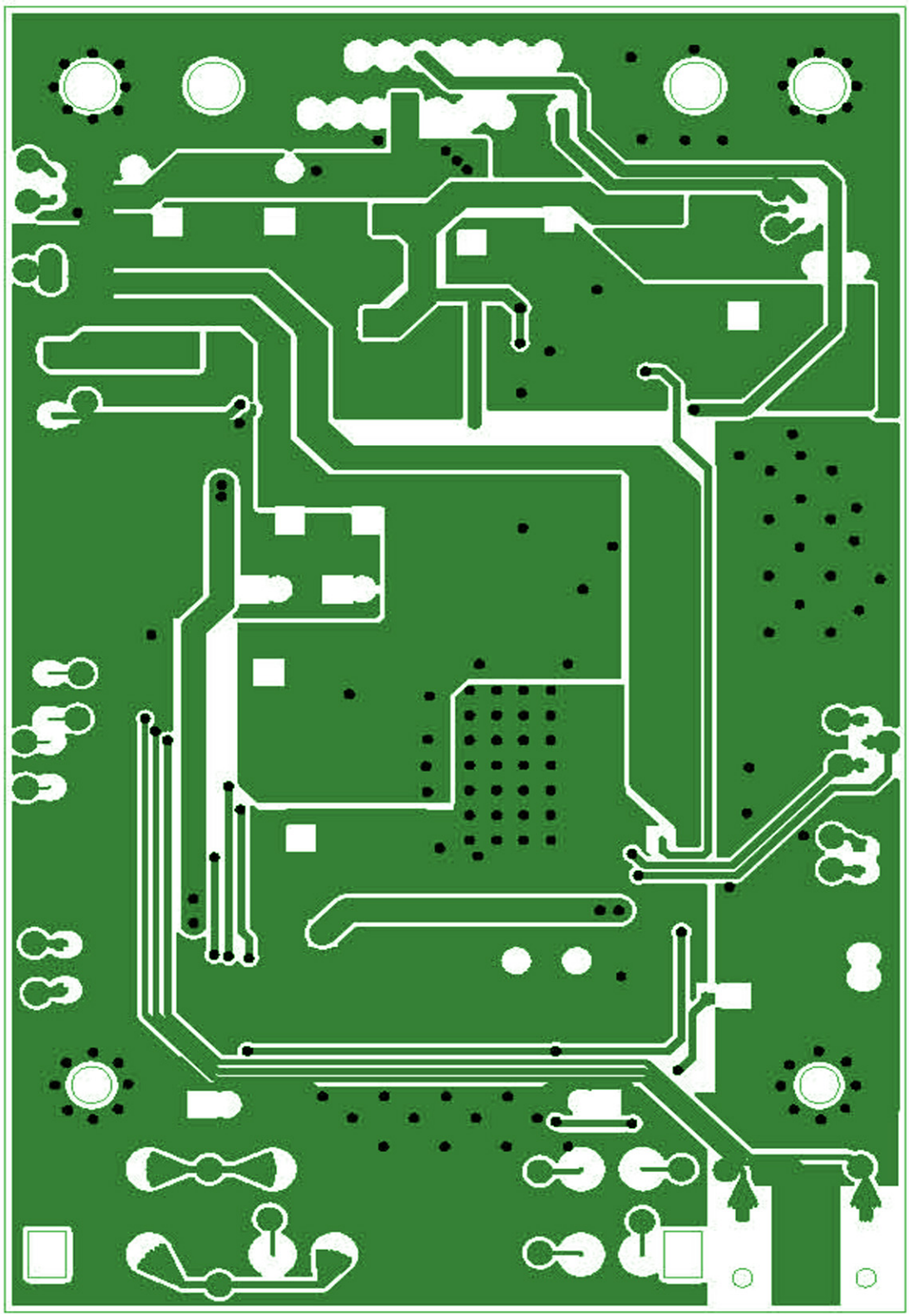
MAIN PCB

MAIN PCB

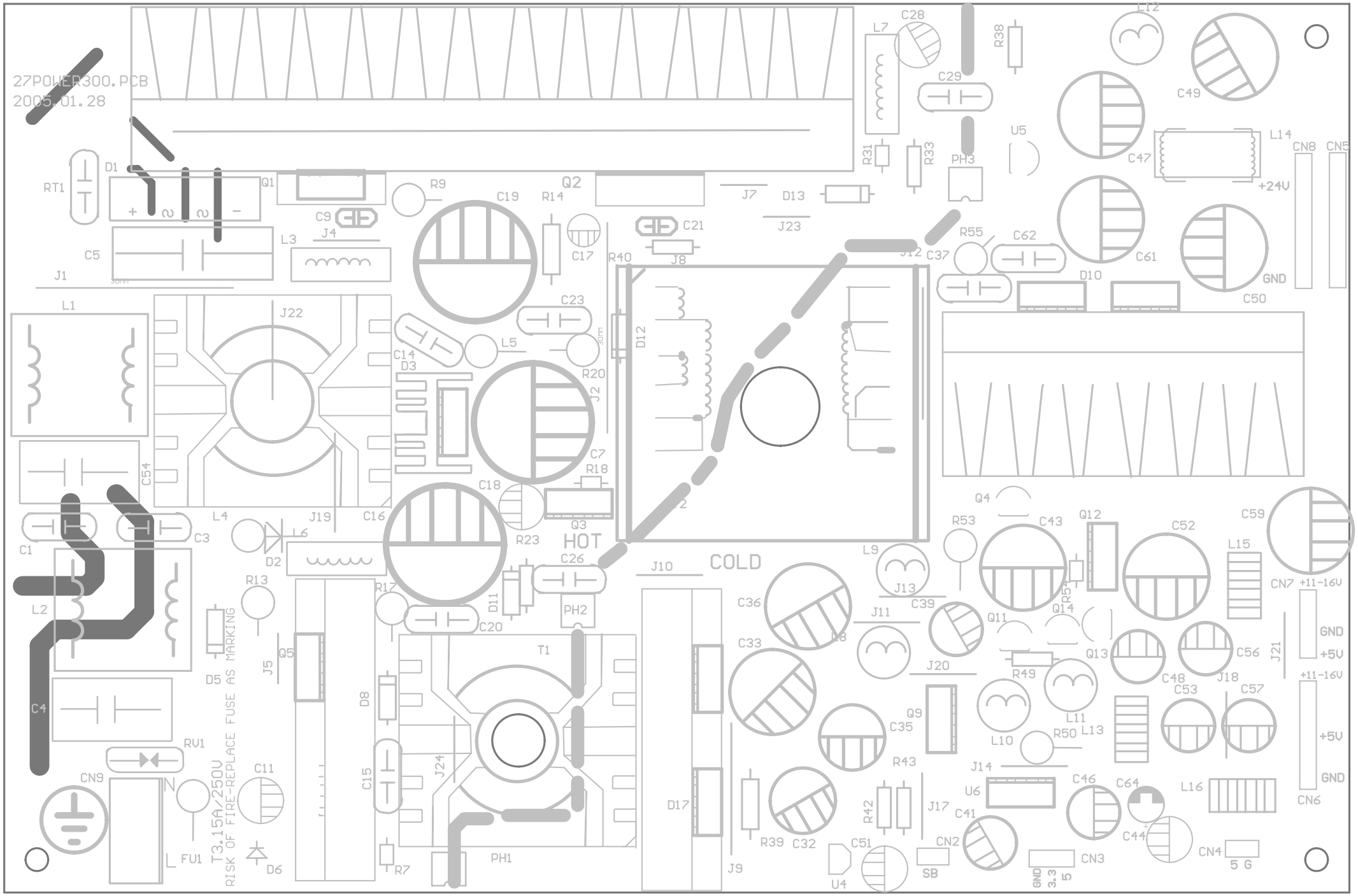


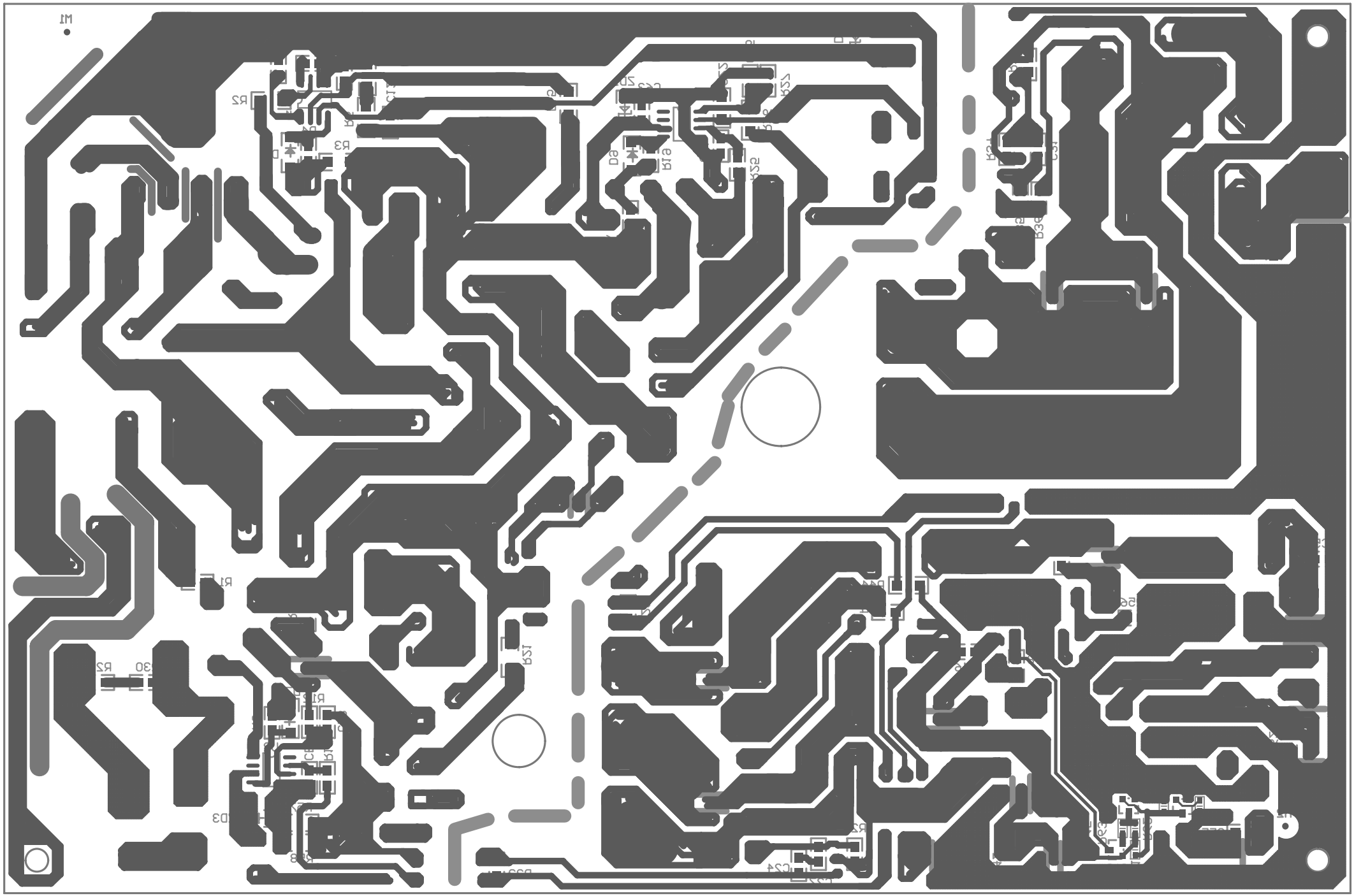
AUDIO PCB

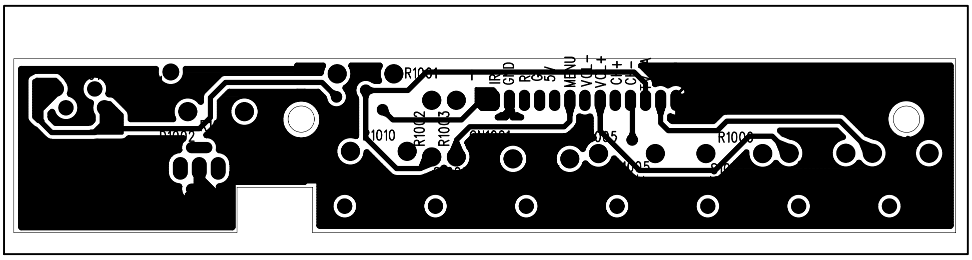

2627SOUND3DO.PCB
2004.10.18
U2
M1
CN8
R37
C41
C57
C36
C43
C19
+12V
C56
C1
VCC
MUTE
L2
C49
C28
IC1
R9
C12
C33
C39
C54
R19
R20
R18
C27
CN10
SCART_R
SCART_L
CN5
SCL
SDA
C52
C37
C31
CN7
C34
C12
CN2
R23
R24
IF
TV-AUDIO
C53
C38
C2
R1
C14
C13
C15
R2
C23
C22
C50
CN6
R14
R12
C60
R25
R27
C55
RCA
M2
PHO



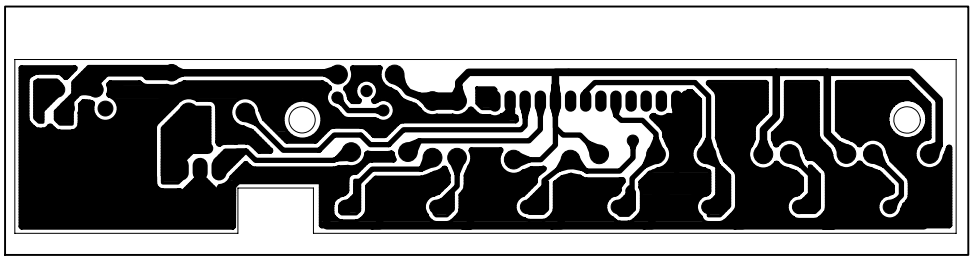
POWER PCB


27POWER300.PCB
2005.01.28
HOT
COLD
T3.15A/250V
RISK OF FIRE-REPLACE FUSE AS MARKING
+24V
GND
+11-16V
+5V
5 G
3.3 5

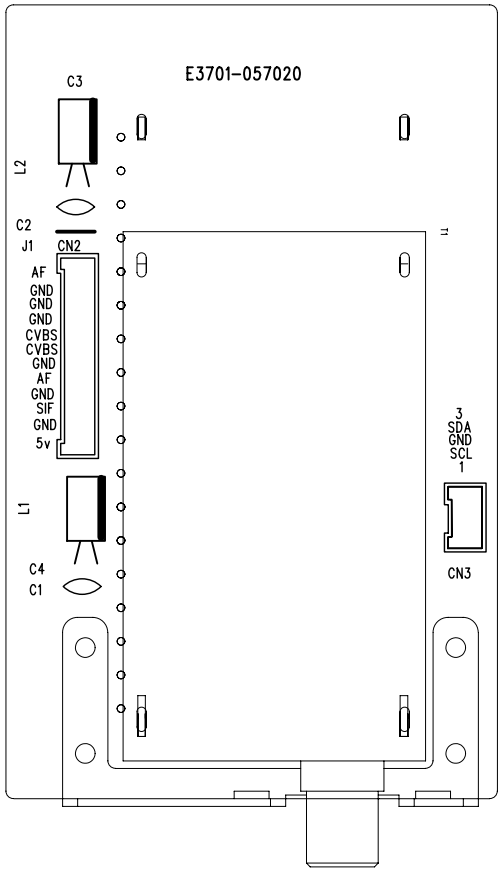


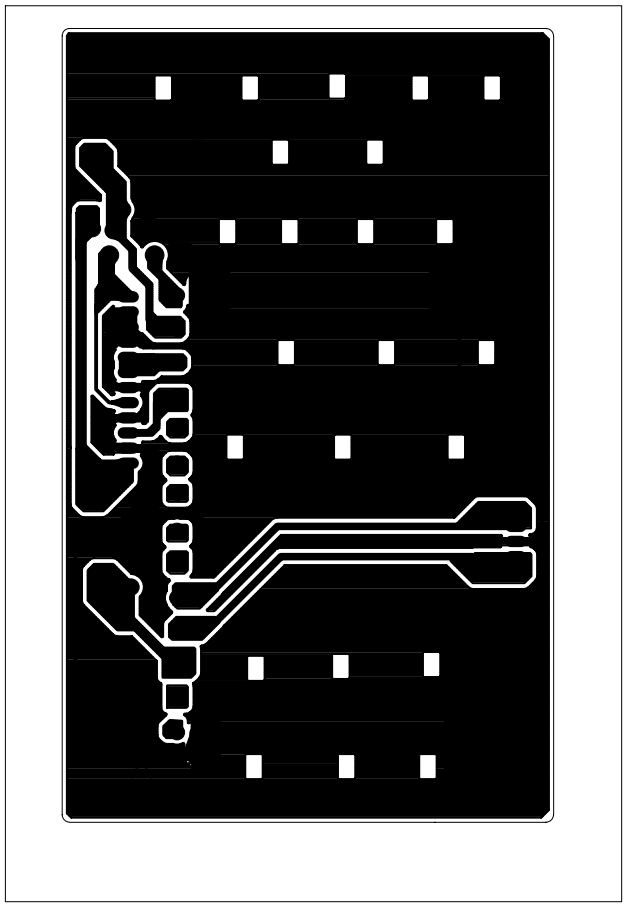


KEY.PCB – Tue Mar 08 10:20:34 2005



TUNER PCB


E3701-057020
C3
L2
C2
J1
CN2
AF
GND
GND
GND
CVBS
CVBS
GND
AF
GND
SIF
GND
5v
L1
C4
C1
3
SDA
GND
SCL
1
CN3



Bill of Material

	TURNER. PCB	1.000	PCB				
413210450RZ00	CAP	2.000	C2, C3				
	50V-104-Z						
414133R10RM00	CAP-EL ϕ 4*7	2.000	C1, C4				
	CD110-10V-33uF-M						
420ET15010920	SOCKET	1.000	CN1				
	DB9						
429EC041010R0	INDOUCTOR	1.000	L1				
	EC0410-100K 10uH 500mA						
4320006000500	WIRE 5mm	2.000	J4, J5				
4320006000750	WIRE 7.5mm	1.000	J3				
4320006001000	WIRE 10mm	1.000	J1				
4320006001250	WIRE 12.5mm	1.000	J2				
442JS6B312110	TUNER JS-6B3121/F2	1.000	TUNER				

7506T2601001F	MTV-2601B POWER PART	1.000					
4110PQ323A000	TRANSFORMER	1.000	T1				
	PQ32/30-40305A						
411EC42405250	TRANSFORMER	1.000	T2				
	KBEC42-40525B						
4121010118J40	CARBON RES	1.000	R7				
	1/8W-100Ω-J						
4121010201J40	CARBON RES	1.000	R53				
	1W-1K-J						
4121010214J40	CARBON RES1/4W-1KΩ	1.000	R49				
4121010314J40	CARBON RES1/4W-10KΩ	1.000	R54				
4121010514J40	CARBON RES1/4W-1MΩ	1.000	R14				
4121010R14J40	CARBON RES1/4W-10Ω	2.000	R23 R33				
4121020214J40	CARBON RES	2.000	R18 R43				
	1/4W-2KΩ-J						

4121024114J40	CARBON RES	1.000	R42				
	RT14-1/4W-240Ω-J						
4121051214J40	CARBON RES1/4W-5.1KΩ	1.000	R39				
4121051314J40	CARBON RES1/4W-51KΩ	1.000	R38				
4123068305J20	METAL OXIDE RES	2.000	R17 R20				
	5W-68K-J						
41230R3305J20	METAL OXIDE RES	1.000	R40				
	RY-5W-0.33Ω-J						
41230R5105J20	METAL OXIDE RES	1.000	R13				
	5W-0.51R-J						
4129008R05A00	HEAT VARIABLE RES 5A 8R	1.000	RT1				
	DIP						
412A07D471K00	PIEZORESISTANCE	1.000	RV1				
	ZOV-07D471K （HEL） DIP						
412A0R5105J00	WIREWOUND RES 5W-0.51Ω-J	1.000	R9				
4130103102M03	HIGH VOLTAGE CERAMIC CAPACITOR	3.000	C14 C23 C20				
	1KV-103-M						

4130151102M00	HIGH VOLTAGE CERAMIC CAPACITOR	3.000	C9 C21,				
	1000V-151-M						
4136104271M02	X CAP	1.000	C4				
	AC275V-104-M（K）						
4136221401M00	Y CAP221 400V	3.000	C1,C3,C26				
4136222251M00	Y CAP	2.000	C29,C37				
	AC250V-222-M（K）						
4136684271M03	X CAP	1.000	C54				
	AC275V-684-M（K）						
4138105401K00	METAL MYLAR CAP	1.000	C5				
	400V-105-K						
4140101451M00	CAP- EL DL:18*35(105°)	2.000	C7 C19				
	CD11G-450V-100u-M						
414110125RM01	CAP-EL 105° high frequency LOW IMPEDANCER	4.000	C11 C17 C18 C28				
	CD11HL 25V-100uF-M						
	CAP-EL 47uF/10V ∮6	1.000	C64				
414110210RM02	CAP-EL 105° high frequency LOW IMPEDANCER	7.000	C41 C44 C46 C51 C53 C56 C57				

	10V-1000uF-M						
414110216RM01	CAP-EL 105° high frequency LOW IMPEDANCER	1.000	C48				
	16V-1000uF-M						
414122225RM01	CAP-EL 105° high frequency LOW IMPEDANCER	8.000	C33 C36 C43 C52 C59 C32 C35 C39				
	25V-2200uF-M						
414133235RM00	CAP-EL 105° high frequency LOW IMPEDANCER	4.000	C47 C49 C50 C61				
	35V-3300uF-M Φ16*31						
414147R451M00	CAP-EL 105°	1.000	C16				
	450V-47uF-M						
4151000015070	CHIP ZENER 1206	1.000					
	15V 0.5W						
415300FR10740	DIODE FR107	1.000	D13（OR 1N4935）				
415301N400720	DIODE（D015）	1.000	D5				
	1N4007						
41530UF400740	DIODE	2.000	D6 D11				
	UF4007						
4153MBR20100C	DIODE MBR20100CT TO-220	1.000	D17				

4153MBR20200C	DIODE MBR20200 TO-220	3.000	D10 D10 D18				
4153MUR180E00	DIODE MUR180E	2.000	D8 D12				
	DO-15						
4153MUR480E00	DIODE MUR480E	1.000	D2				
	DO-35						
4153MUR860T00	DIODE MUR860T	1.000	D3				
	TO-220						
41540KBU6J000	BRIDGE RECTIFIER (DIP) 800V	1.000	D1				
	KBU6J（RS606）						
416000050P030	MOSFET MTP50P03HDL	3.000	Q3 Q9 Q12				
	TO-220						
416002N540100	TRANSISTOR 2N5401	2.000	Q11 Q4				
416002N555100	TRANSISTOR 2N5551	2.000	Q13 Q14				
41602SK265100	MOSFET 2SK2651	1.000	Q5				

416FQP18N5000	MOSFET FQP18N50	1.000	Q1				
	TO-220						
416STW12NK800	MOSFET STW12NK80Z	1.000	Q2				
	TO-3P						
41700000P6210	IC P621[SFH615A-3][PC817]	3.000	PH1 PH2 PH3				
4170000TL4310	IC TL431 DIP TO-92	2.000	U4 U5				
41700DF108410	IC(DIP) DF1084-3.3V	1.000	U6				
	TO-220						
4222500315210	FUSE T3.15A 250V VDE/UL	1.000	FU1				
4290250100040	INDUCTOR 500Ω	4.000	L3 L5 L6 L7				
	（100MHz）						
42903040117B0	INDUCTOR	1.000	L4				
	PQ32/30-40117B						
4290304021600	INDUCTOR	2.000	L1 L2				
	EE25-40216						
42903100K5210	INDUCTOR	2.000	L16 L15				
	T37-52-100K3A						
429035R0K5200	INDUCTOR	1.000	L13				

	T37-52-5R0K						
42903B60974A0	INDUCTOR	1.000	L12				
	DQG-B6-0974A						
42903B61042A0	INDUCTOR	1.000	L9				
	DQG-B6-1042A						
42903B61043A0	INDUCTOR	3.000	L8 L10 L11				
	DQG-B6-1043A						
42903T1605640	INDUCTOR	1.000	L14				
	LCL-T16-0564						
42907RHM40203	magnetic loop	3.000	D3*2, Q1(S)＊1				
	RHM-004002003						
4320007000800	WIRE 8mm Φ0.7	2.000	J7 J23				
4320007001000	WIRE10mm Φ0.7	10.000	J4 J5 J8 J10 J11 J13 J14 J17 J18 R31				
4320007001500	WIRE15mm Φ0.7	4.000	J22 J21 J20 J24				
4320007001700	WIRE17mm Φ0.7	1.000	J19				
4320007002000	WIRE20mm Φ0.7	2.000	J12 J9				

4320007003000	WIRE30mm Φ0.7	1.000	J1				
437T300100260	LEAD WIRE 70mm	1.000	J2				
405T2701050A0	26″POWER300.PCB	1.000					
	2004.8.11						
412700R014J70	CHIP RES 1/4W-0Ω 1206 J	2.000	R57 R58				
412700R01AJ60	CHIP RES 1/10W-0Ω 0805	1.000	C27				
412701021AJ60	CHIP RES 1/10W-1KΩ 0805 J	5.000	R12 R22 R35 R48 R63				
412701031AJ60	CHIP RES 1/10W-10KΩ 0805 J	6.000	R1,R27 R32 R56 R61 R64				
412701041AJ60	CHIP RES 1/10W-100KΩ 0805 J	1.000	R37				
4127010514J70	CHIP RES 1206	1.000	R15				
	1/4W-1M-J						
	CHIP RES 0805	2.000	R3 R24				

	1/4W-1M-J						
4127010R1AJ60	CHIP RES 1/10W-10Ω 0805 J	4.000	R10 R4 R19,R8				
4127012314J70	CHIP RES 1206	1.000	R2				
	1/4W-12K-J						
4127015214J70	CHIP RES 1206	1.000	R44				
	1/4W-1K5-J						
412702021AJ60	CHIP RES 1/10W-2KΩ 0805 J	2.000	R29 R65				
412703011AJ60	CHIP RES 1/10W-300Ω 0805 J	1.000	R25				
412704721AJ60	CHIP RES 1/10W-4.7KΩ 0805 J	1.000	R28				
4127047314J70	CHIP RES 1206	1.000	R3				
	1/4W-47K-J						
412704731AJ60	CHIP RES 1/10W-47KΩ 0805 J	2.000	R11 R16				
412704731AJ70	CHIP RES 1206	1.000	R26				
	1/4W-47K-J						

412705121AJ60	CHIP RES 1/10W-5.1KΩ 0805 J	4.000	R46,R36,R41 R62				
412706221AJ60	CHIP RES 1/10W-6.2KΩ 0805 J	1.000	R34				
4127075R1AJ70	CHIP RES 1/8W-75Ω 1206 J	1.000	R21				
413510150RJ40	CHIP CAP 50V-100P 0805 J NPO	4.000	C13 B1 A1 25				
413510150RJ50	CHIP CAP 1206	1.000	C22				
	50V-100P-J						
413510250RK40	CHIP CAP 0805	1.000	C8				
	50V-102-K						
413510350RK40	CHIP CAP 0805	1.000	C10				
	50V-10nF-K						
413510450RZ40	CHIP CAP 50V-104 0805 Z	10.000	C12 24 31 42 45 55 58 60 62 63				
413522450RZ40	CHIP CAP 50V-224 0805 Z	1.000	C6				
4151000015070	CHIP ZENER 1206	2.000	ZD1 ZD2				
	15V 0.5W						

415201N414870	CHIP DIODE 1N4148 1206	3.000	D4 D9 D7				
41700001377B0	IC NCP1377B	1.000	U3				
	SO8						
4170000332600	IC MC33260D	1.000	U1				
	SO8						
41701203P6010	IC NCP1203D60R2	1.000	U2				
	SOP 8						
	TRANSISTOR 2N5551 SOT23	2.000	Q16 Q17				
	TRANSISTOR 2N5401 SOT23	1.000	Q18				
7516T2601000M	LCDTV-2627 KEY PCB PART	1.000					
40300T1701000	KEY	7.000	P+, P-, V-, V+, MENU, SOURCE, POWER				
	6*6*5mm						
4041920004010	SOCKET 4PIN/2.0	1.000	CN1				
4041920008010	SOCKET 8PIN/2.0	1.000	CN2				
	TVM2627KEY100.PCB	1.000					

	2004.10.6						
4105010300010	LED 3mm GREEN	1.000	LED				
4300000000080	IR	1.000	REMOUT				
7516T2701002F	MTV-2601 TUNER SWITCH PCB	1.000					
4041920002010	SOCKET 2PIN/2.0	2.000	CN4,6				
4041920003010	SOCKET 3PIN/2.0	3.000	CN1,2,3				
4041920005010	SOCKET 5PIN/2.0	1.000	CN5				
	2627-TURNER300.PCB	1.000					
	2004.10.18						
414147116RM00	CAP-EL φ8*12	1.000	C1				
	CD110-16V-470uF-M						
420ET15010910	SOCKET	1.000	DB2				
	DB-9A						
420ET15010920	SOCKET	1.000	DB1				
	DB9						

4320005001000	WIRE 10mm	2.000	J1、J2				
	MTV-2701mainboard	0.000					
4041920002010	SOCKET 2PIN/2.0	3.000	CN5,CN3,CN13				
4041920003010	SOCKET 3PIN/2.0	3.000	CN9,CN11,CN2				
4041920004010	SOCKET 4PIN/2.0	1.000	CN6				
4041920005010	SOCKET 5PIN/2.0	1.000	CN14				
4041920006010	SOCKET 6PIN/2.0	1.000	CN12				
4041920007010	SOCKET 7PIN/2.0	1.000	CN10				
4041920008010	SOCKET 8PIN/2.0	1.000	POWER1				
4041920010010	SOCKET 10PIN/2.0	1.000	KBD1				
414110116RM00	CAP-EL 16V-100uF M φ6*7	13.000	C168,C217, C220,C225,C226,C231,C246,C250,C10,23,C62,				
			C208,C249				
414110210RM00	CAP-EL	2.000	C197,C227				
	10V-1000uF-M						
414110R16RM00	CAP-EL	3.000	C45-C47				
	16V-10uF-M						
41412R216RM00	CAP-EL	1.000	C233				

	16V-2.2uF-M						
414147116RM00	CAP-EL	5.000	C124,C219,C221,C223,224				
	CD110-16V-470uF-M						
414147125RM00	CAP-EL 25V-470uF M≤φ8*15	1.000	C222				
414147R16RM00	CAP-EL 16V-47uF Mφ5*7	12.000	C165-167,196 C209-C216				
417000078L050	IC 78L05	1.000	IC9				
4202T27012010	AV SOCKET	1.000	RCA1				
	AV3-8.4-20						
4202T30011210	RCA SOCKET AV8-8.4-7	1.000	RGA				
420AD10006110	S-SOCKET DSW-06P	1.000	S-VIDEO				
420DT15011510	SOCKET	1.000	VGA				
	DB-15						
424000006101A	OSCILLATOR〈49S〉-10℃---80℃	1.000	X3				
	10M(+-20PPM,20PF)						
424000256201A	OSCILLATOR<49S>-10℃---80℃	1.000	X1				
	20.25M(+-20PPM,20PF)						
424003186142A	OSCILLATOR〈49S〉-10℃---80℃	1.000	X4				
	14.31818M(+-15PPM,20PF)						
405T2701A5302	2627A-pixwork300 PCB	1.000					
	MAINBOARD（04.12.17）						
4105010300060	LED-CHIP GREEN 0805	1.000	LED1				
	SA0805G1C-1A-01						
412700R014J70	CHIP RES 1/4W-0Ω 1206 J	1.000	L29				

412700R01AJ80	CHIP RES 1/10W-0Ω 0603J	22.000	R14,R40,R28,R81,R82,R142,R143,R178,187,R233,R245-250,				
			R41,R66,C254-C256,R97				
412701011AJ80	CHIP RES 1/10W-100Ω 0603 J	1.000	R59				
412701021AJ80	CHIP RES 1/10W-1KΩ 0603 J	5.000	R2,R134,R188,R190,R226				
412701031AF80	CHIP RES 1/10W-10K 0603 F	2.000	R232,R73				
412701031AJ80	CHIP RES 1/10W-10KΩ 0603 J	19.000	R29-30,R118,119 R159-169,179 183,191 R228				
412701221AJ80	CHIP RES 1/10W-1.2KΩ 0603 J	1.000	R71				
412702011AJ80	CHIP RES 1/10W-200Ω 0603 J	3.000	R116,R117,R153				
412702021AJ80	CHIP RES 1/10W-2KΩ 0603 J	7.000	R44-R48,R170,R49				
412702221AJ80	CHIP RES 1/10W-2.2KΩ 0603 J	2.000	R36,R37				
412702231AJ80	CHIP RES 1/10W-22KΩ 0603 J	1.000	R63				
412702251AJ80	CHIP RES 0603	2.000	R93,R130				
	1/10W-2.2M-J						
4127022R1AJ80	CHIP RES 1/10W-22Ω 0603 J	2.000	R34,R35				
412703011AJ80	CHIP RES 1/10W-300Ω 0603 J	4.000	R92,R128,R129,R174				
412703321AJ80	CHIP RES 1/10W-3.3KΩ 0603 J	26.000	R90,R91,R104-R111,R135-R137,R144-R148,R171-R173,R227				
			,R234,238,R253,R255				

412704711AJ80	CHIP RES 1/10W-470Ω 0603 J	11.000	R132,R133,R60,R61,R67-R69,R192-R194,L43				
4127047R1AJ80	CHIP RES 1/10W-47Ω 0603 J	14.000	R13,R87,R88,R89,R112-R115,R138,R141,R64,R101,R102,				
			R103				
412705121AJ80	CHIP RES 1/10W-5.1KΩ 0603 J	1.000	R252				
412705621AJ80	CHIP RES 1/10W-5.6KΩ 0603 J	1.000	R62				
412706811AJ80	CHIP RES 1/10W-680Ω 0603 J	3.000	R38,R39,R175				
412706821AJ80	CHIP RES 1/10W-6.8KΩ 0603 J	3.000	R131,R75,R254				
4127075R1AJ80	CHIP RES 1/10W-75Ω 0603 J	18.000	R50-R57,R58,R94-R96,R98-R100,R184,R74,R76				
413510250RK60	CHIP CAP 0603	5.000	C31-C34,C137				
	50V-102-K						
413510450RZ60	CHIP CAP 50V-104 0603 Z	110.000	C2,C4-6,C9,C11-19,C48-53,C81-97,C99-110,C114-123,				
			C138-142,155-156 C169-C179,C181-185,C188-C190,				
			C126-129,C131,C63,C65,C67,C258				
			C192-C195,C198-C207,C232,C234				
413510R50RJ60	CHIP CAP 50V-10P 0603 J NPO	5.000	C111,C143,C144,C180,C228				
413520R50RJ60	CHIP CAP 50V-20P 0603 J NPO	9.000	C58-59,C112,113,186,187,146,147,148				
413522416RZ60	CHIP CAP 16V-0.22u 0603 Z	8.000	C36-C40,C72,C73,C74				
413522R50RJ60	CHIP CAP 50V-22P 0603 J NPO	2.000	C25,C26				
413533150RK60	CHIP CAP 50V-330P 0603 K	4.000	C55-C57,C75				

413533R50RJ60	CHIP CAP 50V-33P J 0603 NPO	3.000	C69,C70,C71				
413539250RK60	CHIP CAP 50V-392 0603 K	1.000	C132				
413539350RZ60	CHIP CAP 0603	1.000	C136				
	50V-39nF-Z						
413547350RZ60	CHIP CAP 0603	6.000	C42-C44,C133-C135				
	50V-47n-Z						
413568250RK60	CHIP CAP 0603	1.000	C77				
	50V-6.8nF-K						
413568350RZ60	CHIP CAP 50V-0.068μ 0603 Z	1.000	C78				
413568410RZ60	CHIP CAP 0603	4.000	C27-C30				
	10V-0.68uF-Z						
415200BAV9960	DIODE (SOT-23B)	7.000	D1-D7				
	BAV99						
415201N414870	IODE 1N4148 1206	6.000	D11-13,17,18,D15				
4160000901421	CHIP TRANSISTOR(SOT23)	6.000	Q3-7,Q10				
	9014 NPN						
4160000901520	CHIP TRANSISTOR 9015	1.000	Q16				
416PCHAN20P03	MOSFET P-CHANNEL TO-252	1.000	Q8				
	MTD20P03HDLT4 OR 25P03						
417000024C320	IC(SO8)	1.000	U5				
	24C32						
4170000AC3200	IC(SO14)	1.000	UD				
	AC32						

4170000LM3580	IC(SO-8)	1.000	UE				
	LM358						
41700074HC140	IC 74HC14[SOP]	1.000	U3				
417000HC37400	IC(SSOP20)	1.000	U2				
	HC374						
4170074LV1260	IC(SO14)	2.000	UB UA				
	SN74LV126						
41700AMS11170	IC AMS1117[SOP]3.3V	2.000	IC7,IC8				
41700APL11170	IC APL1117ADJ[SOT-223]	2.000	IC2,IC5				
41700Z8622910	IC Z86229 SO18	1.000	U7				
41704M000161A	IC(TSOP54) HY57V641620HG	1.000	U9				
	4M*16 SDRAM 7ns						
4170LV800DT10	IC(TSOP48)	1.000	U18				
	AM29LV800DT-90EC						
4170LVC162440	IC (TSSOP48)	2.000	U14, U15				
	LVC16244						
4170MAX232A00	IC (SO16)	1.000	U12				
	MAX232A						
4170MST988310	IC(LQFP80)	1.000	U11				
	MST9883B-C(/110)						
41763LVDM8310	IC THC63LVDM83A	1.000	U19				
	THINE						
417AZ1084S3V3	IC(TO-263)	1.000	IC4				
	AZ1084S-3.3V						
417FSAV330M10	IC(SO16)	1.000	U10				
	P15V330/FSAV330M						
417PW11320Q10	IC PW113-20Q [PQFP208]	1.000	U17				

417PW12350010	IC PW1235 [PQFP256]	1.000	UC				
417SOHCF40520	IC HCF4052 SOP	1.000	U21				
417VPC3230D10	IC VPC3230D PQFP80	1.000	U4				
420FT15013010	SOCKET SOP	1.000	CON1				
	DF14-30S-1.25C						
42847R0082010	CHIP RES 0603	20.000	RP7-RP20 RP33-38				
	47Ω*4						
429025R6K0010	CHIP INDUCTOR 1210	5.000	L8 24 27 30 36				
	DR43-5R6K						
429042R2J7010	CHIP INDUCTOR 1210	10.000	21-23 26 31 33-35 37,L41				
	ALM322522-2R2K						
429043R3J5010	CHIP INDUCTOR 1206	1.000	L42				
	3.3uH-J						
429043R3J8011	CHIP INDUCTOR 0603	5.000	L9-L11,L39,L38				
	3.3uH-J						
4290511R08010	CHIP INDUCTOR 0603	7.000	L12-17,44				
	11 OHM@100MHz						
4290512108010	CHIP INDUCTOR 0603	1.000	R11				
	BK1608HM121-T						
4290550108010	CHIP INDUCTOR 500Ω 0603	1.000	R86				
7596T2701003F	2601B SOUND PCB	1.000					
4041920002010	SOCKET 2PIN/2.0	5.000	CN3,CN6-CN9				

4041920003010	SOCKET 3PIN/2.0	1.000	CN2				
4041920004010	SOCKET 4PIN/2.0	1.000	CN5				
4041920005010	SOCKET 5PIN/2.0	1.000	CN1				
4041920006010	SOCKET 6PIN/2.0	1.000	CN10				
4121010214J40	CARBON RES 1/4W-1KΩ	4.000	R35-R38				
414022125RM00	CAP-EL 25V-220uF M	1.000	C42				
41404R716RM00	CAP-EL 16V-4.7uF M	1.000	C47				
414110116RM00	CAP-EL 16V-100uF M Φ6*7	5.000	C49 C55 C59 C60 C61				
414110R16RM00	CAP-EL	6.000	C16-21				
	16V-10uF-M						
414122R16RM00	CAP-EL Φ5*11	1.000	C48				
	CD110-16V-22uF-M						

414147125RM00	CAP-EL 25V-470uF M≦Φ8*15	7.000	C1,C41,C43,C56,57,58,C51				
415201N414840	DIODE 1N4148	1.000	D1				
417TDA8947J10	IC TDA8947J SOT243-1	1.000	U2				
4202T30011310	RCA SOCKET	1.000	RCA				
	AV6-8.4-20						
4204T15010310	EAR SOCKET	1.000	PHO				
	EJ-0357-3P						
424004326183A	OSCILLATOR49S -10℃---80℃	1.000	X1				
	18.432MHz ±15PPM, 15P						
405T2701059B0	2627SOUND300.PCB	1.000					
412700R01AJ80	CHIP RES 1/10W-0Ω 0603J	1.000	R26				
412701021AJ80	CHIP RES 1/10W-1KΩ 0603 J	5.000	R1,R2,R24,R27,R33				
412701031AJ80	CHIP RES 1/10W-10KΩ 0603 J	6.000	R3,R7,R8,R25,R29,R34				

412702021AJ80	CHIP RES 1/10W-2KΩ 0603 J	1.000	R30				
412702211AJ80	CHIP RES 1/10W-220Ω 0603 J	1.000	R12				
412702231AJ80	CHIP RES 1/10W-22KΩ 0603 J	1.000	R4				
412703021AJ80	CHIP RES 1/10W-3KΩ 0603 J	3.000	R6,R9,R13				
412704731AJ80	CHIP RES 1/10W-47KΩ 0603 J	4.000	R18-R21				
4127047R1AJ80	CHIP RES 1/10W-47Ω 0603 J	1.000	R14				
412705121AJ80	CHIP RES 1/10W-5.1KΩ 0603 J	2.000	R31 R32				
412705611AJ80	CHIP RES 1/10W-560Ω 0603 J	1.000	R10				
412705621AJ80	CHIP RES 1/10W-5.6KΩ 0603 J	1.000	R28				
413510150RJ60	CHIP CAP 50V-100P 0603 J NP0	1.000	C2				

413510250RK60	CHIP CAP 0603	2.000	C26,C27				
	50V-102-K						
413510425RZ60	CHIP CAP 25V-104 0603 Z	11.000	C3,C28-C36,C40				
413515250RK60	CHIP CAP 50V-1500P 0603 K	3.000	C52-C54				
413520R50RJ60	CHIP CAP 50V-20P 0603 J NPO	2.000	C22,C23				
413533416RZ60	CHIP CAP 0603	9.000	C4-C12				
	16V-0.33uF-Z						
413547150RK60	CHIP CAP 50V-470P 0603 K	3.000	C37-C39				
413556R50RJ60	CHIP CAP 50V-56P 0603 J NPO	3.000	C13-C15				
4160000901421	CHIP CAP (SOT23)	6.000	Q3,Q5,Q6,Q1,Q7,Q8				
	9014 NPN						
4160000901520	CHIP TRANSISTOR 9015	1.000	Q4				

41700APL11170	IC APL1117ADJ[SOT-223]	1.000	IC1				
417MSP3450G10	IC MSP3450G-QA-C12-001	1.000	U1				
	[PQFP80]						
429025R6K0010	CHIP INDUCTOR 1210	1.000	L2				
	DR43-5R6K						
429042R2J7010	CHIP INDUCTOR 1210	2.000	L3,L4				
	ALM322522-2R2K						

IC SPECIFICATION

-PW113 (Top View)
-PW1235
-MST9883B
-Z86229
-THC63LVDM83R
-MSP34XOG
-TDA8947J
-VPC323XD

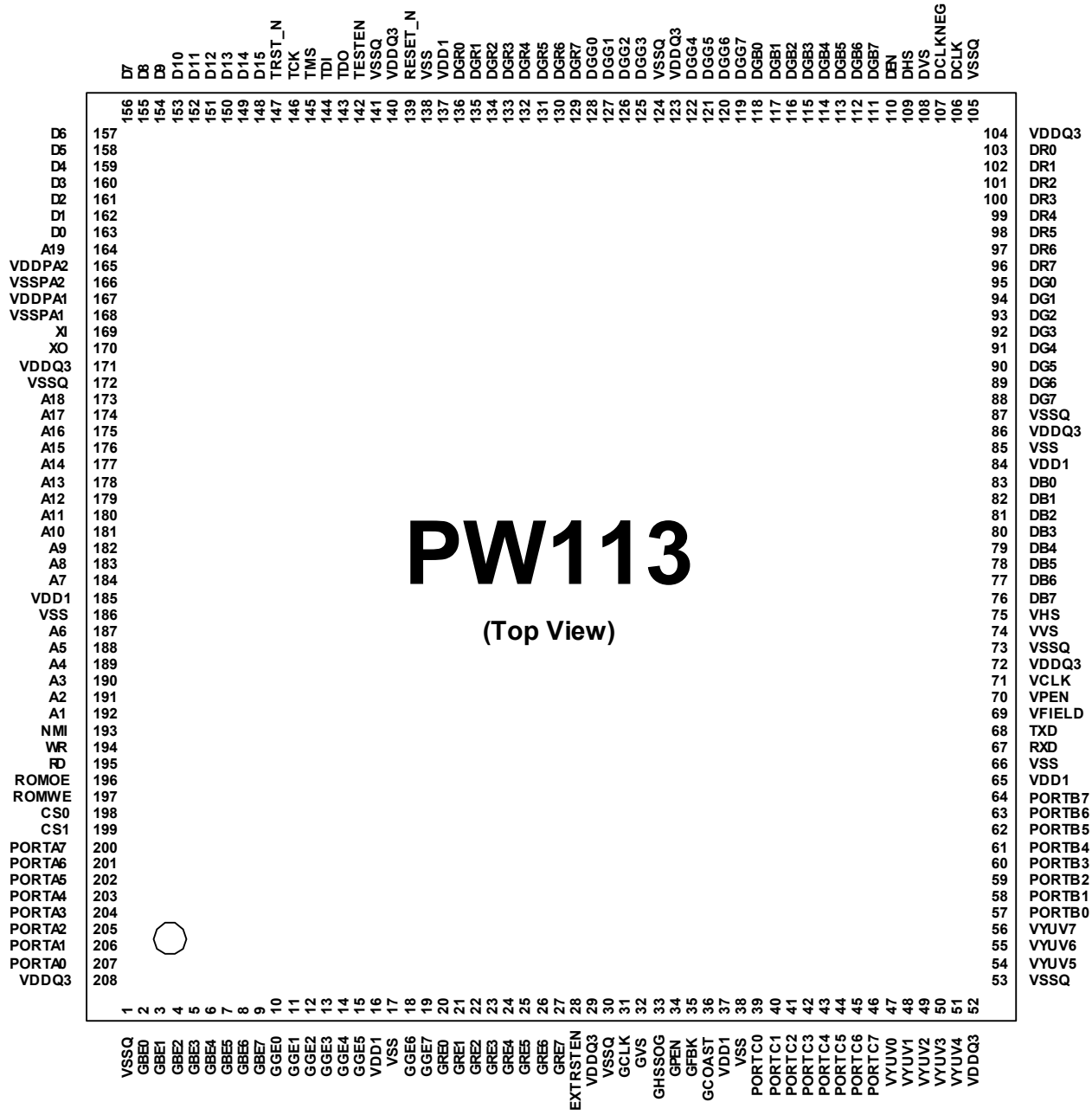


Figure 2-1 Pin Locations

2.3 Pin Descriptions

Table 2-1 provides detailed Video Port pin descriptions.

Table 2-1 Video Port Pin Descriptions

Name	Pin(s)	Type	Function
VCLK	71	ID 5	VPort Pixel Clock. The VCLK pin is used for video port image capture. The polarity can be selected by the VCLKPOL bit.
VVS	74	ID 5	VPort Vertical Sync. Indicates start of next field or frame of input data. This signal is internally polarity corrected so VVS can be either active-high or active-low. The current status of the VVS signal is given by VPOL and VSOK status bits when the video port is selected by the PORTSEL bit. VVS is not used when a composite digital sync source is used (COMPEN). VVS is required in ITUR656 input mode.
VHS	75	ID 5	VPort Horizontal Sync. Indicates start of next line of data input. This signal is internally polarity corrected and monitored for composite sync content. The current status of the GHS signal is given by the HPOL, HSOK & COMP status bits when the video port is selected by the PORTSEL bit. VHS can supply horizontal sync information or digital composite sync information depending on the COMPEN bit. VHS is required in ITUR656 input mode.
VPEN	70	ID 5	VPort Pixel Enable. Used when external flow control capture mode is enabled by the EXTFCE bit. When VPEN is active, the input data is valid. The polarity can be selected by the PENPOL bit. Use of this pin allows non-contiguous input data.
VFIELD	69	ID 5	VGPort Field Input. Video or Graphics port odd/even field indicator specifies whether odd or even field of interlaced input is being captured.This pin is enabled by the FLDSEL bit and the polarity can be specified by the FLDINV bit. Field information can also be derived from VVS and VHS, so VFIELD is not required in some applications.

Table 2-2 provides detailed Graphics Port pin descriptions.

Table 2-2 Graphics Port Pin Descriptions

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>GCLK</td><td>31</td><td>ID 5</td><td>GPort Pixel Clock. The GCLK pin is used for graphics port image capture. The polarity can be selected by the GCKPOL bit.The GCLK input can be disabled by the GCLKOFF bit to reduce power consumption.</td></tr>
<tr><td>GVS</td><td>32</td><td>ID 5</td><td>GPort Vertical Sync. Indicates start of next field or frame of data. This signal is internally polarity corrected so GVS can be either active-high or active-low. The current status of the GVS signal is given by VPOL and VSOK status bits when the graphics port is selected by the PORTSEL bit. GVS is not used when a composite digital sync source is used which can be specified by the SOGSEL and COMPEN bits.</td></tr>
<tr><td>GPEN</td><td>34</td><td>ID 5</td><td>GPort Pixel Enable. Used when external flow control capture mode is enabled by the EXTFCE bit. When GPEN is active, the input data is valid. The polarity can be selected by the GPENPOL bit. Use of this pin allows non-contiguous input data.</td></tr>
<tr><td>GHSSOG</td><td>33</td><td>ID 5</td><td>GPort Horizontal Sync/GPort Sync-on-Green. This pin has two different functions depending on the SOGSEL bit:
<table>
<tr><th>SOGSEL</th><th>GHSSOG Function</th></tr>
<tr><td>0</td><td>GHS: GPort Horizontal Sync. Indicates the start of the next line of input data. This signal is internally polarity corrected and monitored for composite sync content. The current status of the GHS signal is given by the HPOL, HSOK & COMP status bits when the graphics port is selected by the PORTSEL bit. GHS can supply horizontal sync information or digital composite sync information depending on the COMPEN and SOGSEL bits.</td></tr>
<tr><td>1</td><td>SOG: Pin is sync-on-green. Driven by an external sync stripper circuit, this pin is monitored (SOGACT status bit) and can supply composite sync information (depending on SOGSEL & COMPEN bits).</td></tr>
</table></td></tr>
<tr><td>GCOAST</td><td>36</td><td>OS</td><td>GPort PLL Coast. Tells the PLL when to coast (ignore GREF) during vertical blanking. Used to prevent the PLL from reacting to extra or missing HS pulses during vertical blanking. Coast duration and polarity is programmable through the PLLCM, PLLCB & PLLCE bits.</td></tr>
<tr><td>GFBK</td><td>35</td><td>ID 5</td><td>GPort PLL Feedback / Line Advance Input.
• When PORTSEL=0, this pin is not used.
• When PORTSEL=1, this pin has two different functions depending on the EXTFCE bit:
<table>
<tr><th>EXTFCE</th><th>GFBK Function</th></tr>
<tr><td>0</td><td>GFBK: An input that is typically driven by the FBK output of an ADC/PLL device. In free running capture mode this signal is used to define the horizontal capture region (along with the CAPL and CAPW registers), and advances the GPort capture controller to the next input line. The LAVPOL bit is used to select the polarity of GFBK.</td></tr>
<tr><td>1</td><td>GLAV: An input to the graphics port line advance. Used in external flow control capture mode. When GLAV transitions (depending on LAVPOL and LAVMOD bits), the GPort capture controller advances to the next input line.</td></tr>
</table></td></tr>
</table>

Table 2-2 Graphics Port Pin Descriptions (continued)

Name	Pin(s)	Type	Function
GRE0	20	ID 5	GPort Red Pixel Data. GPort Red Even Pixel Data when in 48-bit input mode.
GRE1	21	ID 5	
GRE2	22	ID 5	
GRE3	23	ID 5	
GRE4	24	ID 5	
GRE5	25	ID 5	
GRE6	26	ID 5	
GRE7	27	ID 5	
GGE0	10	ID 5	GPort Green Pixel Data. GPort Green Even Pixel Data when in 48-bit input mode.
GGE1	11	ID 5	
GGE2	12	ID 5	
GGE3	13	ID 5	
GGE4	14	ID 5	
GGE5	15	ID 5	
GGE6	18	ID 5	
GGE7	19	ID 5	
GBE0	2	ID 5	GPort Blue Pixel Data. GPort Blue Even Pixel Data when in 48-bit input mode.
GBE1	3	ID 5	
GBE2	4	ID 5	
GBE3	5	ID 5	
GBE4	6	ID 5	
GBE5	7	ID 5	
GBE6	8	ID 5	
GBE7	9	ID 5	

Table 2-3 provides detailed Display/Graphics Port pin descriptions.

Table 2-3 Display/Graphics Port Pin Descriptions

Name	Pin(s)	Type	Function
DGR0	136	I/O SR5	DGPort Red Pixel Data. In dual pixel output mode these pins are the ODD red outputs. In single pixel output mode these pins are not used.
DGR1	135	I/O SR5	
DGR2	134	I/O SR5	
DGR3	133	I/O SR5	
DGR4	132	I/O SR5	
DGR5	131	I/O SR5	
DGR6	130	I/O SR5	
DGR7	129	I/O SR5	

Table 2-3 Display/Graphics Port Pin Descriptions (continued)

Name	Pin(s)	Type	Function
DGG0	128	I/O SR5	DGPort Green Pixel Data. In dual pixel output mode these pins are the ODD green outputs. In single pixel output mode these pins are not used.
DGG1	127	I/O SR5	
DGG2	126	I/O SR5	
DGG3	125	I/O SR5	
DGG4	122	I/O SR5	
DGG5	121	I/O SR5	
DGG6	120	I/O SR5	
DGG7	119	I/O SR5	
DGB0	118	I/O SR5	DGPort Blue Pixel Data. In dual pixel output mode these pins are the ODD blue outputs. In single pixel output mode these pins are not used.
DGB1	117	I/O SR5	
DGB2	116	I/O SR5	
DGB3	115	I/O SR5	
DGB4	114	I/O SR5	
DGB5	113	I/O SR5	
DGB6	112	I/O SR5	
DGB7	111	I/O SR5	

Table 2-4 provides detailed Display Port pin descriptions.

Table 2-4 Display Port Pin Descriptions

Name	Pin(s)	Type	Function
DCLK	106	OSR	DPort Pixel Clock. Output clock for the display port pixel data. DCLK is enabled by the DCLKEN bit and can be inverted by the DCPOL bit. DCLK can be set to run at ½ pixel rate, for dual pixel output mode, by setting the DCK2EN bit. The DCLK output can be disabled by the DCLKOFF bit to reduce power consumption.
DCLKNEG	107	OSR	• DPort Pixel Clock.
DVS	108	OS	DPort Vertical Sync. DVS can be either active-high or active-low depending on the VSPOL bit. Width and timing is controlled by the VPLSE and VDLY registers.
DHS	109	OS	DPort Vertical Sync. DHS can be either active-high or active-low depending on the HSPOL bit. Sync width can be controlled by the HPLSE register.

Table 2-4 Display Port Pin Descriptions (continued)

Name	Pin(s)	Type	Function
DEN	110	OS	DPort Pixel Enable. This signal is active whenever valid data is present. The polarity is specified by the DENPOL bit.
DR0	103	OSR	DPort Red Pixel Data. In dual pixel output mode these pins are the EVEN red outputs.
DR1	102	OSR	
DR2	101	OSR	
DR3	100	OSR	
DR4	99	OSR	
DR5	98	OSR	
DR6	97	OSR	
DR7	96	OSR	
DG0	95	OSR	DPort Green Pixel Data. In dual pixel output mode these pins are the EVEN green outputs. These pins can also be used in conjunction with the PORTB pins for higher color depth.
DG1	94	OSR	
DG2	93	OSR	
DG3	92	OSR	
DG4	91	OSR	
DG5	90	OSR	
DG6	89	OSR	
DG7	88	OSR	
DB0	83	OSR	DPort Blue Pixel Data. In dual pixel output mode these pins are the EVEN blue outputs.
DB1	82	OSR	
DB2	81	OSR	
DB3	80	OSR	
DB4	79	OSR	
DB5	78	OSR	
DB6	77	OSR	
DB7	76	OSR	

Table 2-5 provides detailed Microprocessor Interface pin descriptions.

Table 2-5 Microprocessor Interface Pin Descriptions

Name	Pin(s)	Type	Function
WR	194	I/O D5	Write Enable. Low indicates a write to external RAM or other devices.
RD	195	I/O D5	Read Enable. Low indicates a read to external RAM or other devices.
ROMOE	196	OS	ROM Output Enable. Low output indicates a read from external ROM.
ROMWE	197	OS	ROM Write Enable. Low indicates a write to external ROM.
CS0	198	I/O D5	Miscellaneous Chip Select 0. Low selects external devices.
CS1	199	I/O D5	Miscellaneous Chip Select 1. When EXTRAMEN=0, low selects external devices. Chip select for external RAM. When EXTRAMEN=1, low selects external RAM. (RAMCS)
NMI	193	ID 5	Non-Maskable Interrupt. A high input triggers a non-maskable interrupt to the on-chip microprocessor.
A1	192	I/O D5	Microprocessor address bus output bits (19:1).
A2	191	I/O D5	
A3	190	I/O D5	
A4	189	I/O D5	
A5	188	I/O D5	
A6	187	I/O D5	
A7	184	I/O D5	
A8	183	I/O D5	
A9	182	I/O D5	
A10	181	I/O D5	
A11	180	I/O D5	
A12	179	I/O D5	
A13	178	I/O D5	
A14	177	I/O D5	
A15	176	I/O D5	
A16	175	I/O D5	
A17	174	I/O D5	
A18	173	I/O D5	
A19	164	I/O D5	

Table 2-5 Microprocessor Interface Pin Descriptions (continued)

Name	Pin(s)	Type	Function
D0	163	I/O D5	Microprocessor 16-bit bidirectional data bus.
D1	162	I/O D5	
D2	161	I/O D5	
D3	160	I/O D5	
D4	159	I/O D5	
D5	158	I/O D5	
D6	157	I/O D5	
D7	156	I/O D5	
D8	155	I/O D5	
D9	154	I/O D5	
D10	153	I/O D5	
D11	152	I/O D5	
D12	151	I/O D5	
D13	150	I/O D5	
D14	149	I/O D5	
D15	148	I/O D5	

Table 2-6 provides detailed Peripheral Interface pin descriptions.

Table 2-6 Peripheral Interface Pin Descriptions

Name	Pin(s)	Type	Function
PORTA0	207	I/O U5	General-purpose I/O port bit controlled by PADAT0 and PAEN0. This pin has one other possible function when EXTRAMEN=1. When EXTRAMEN=1 and PAEN0=0, PORTA1 is microprocessor address bit 0 (A0).
PORTA1	206	I/O U5	General-purpose I/O port bit controlled by PADAT1 and PAEN1. This pin has one other possible function when EXTRAMEN=1. When EXTRAMEN=1 and PAEN1=0, PORTA1 is microprocessor byte-high enable (BHEN)
PORTA2	205	I/O U5	General-purpose I/O port bit controlled by PADAT2 and PAEN2. This pin has one other possible function when GREFEN=1. When GREFEN=1 and PAEN2=0, PORTA2 is GPort PLL reference out, a delayed version of internal horizontal sync (typically connected to the external PLLs reference input) (GREF)
PORTA3	204	I/O U5	General-purpose I/O port bit controlled by PADAT3 and PAEN3. This pin can also function as an external clock source for DCLK (DCLKEXT) when the internal PLLs are disabled.
PORTA4	203	I/O U5	General-purpose I/O port bit controlled by PADAT4 and PAEN4. This pin has one other possible function when IREN=1. When IREN=1 and PAEN4=1, this pin can function as an input to the on-chip IR receiver 0. (IRRCVR0)

Table 2-6 Peripheral Interface Pin Descriptions (continued)

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>PORTA5</td><td>202</td><td>I/O U5</td><td>General-purpose I/O port bit controlled by PADAT5 and PAEN5. This pin has other possible functions depending on the IREN, EIEN registers.
• When EIEN=1 and PAEN5=1, this pin can function as an external interrupt to the on-chip CPU.
• When IREN=1 and PAEN5=1, this pin can function as an input to the on-chip IR receiver 1. (IRRCVR1). .</td></tr>
<tr><td>PORTA6</td><td>201</td><td>I/O U5</td><td>General-purpose I/O port bit controlled by PADAT6 and PAEN6. This pin can also function as BLKSPL when BLKSMPLEN=1.
• When BLKSMPLEN=1 and PAEN6=0, PORTA6 is GPORT black sample clamp pulse output (typically used as port of an external DC restoration circuit) (BLKSPL) This pin has one other possible function when PREF1EN=1.
• When PREF1EN=1 and PAEN6=0, PORTA6 is a variable duty-cycle pulse reference generator (PWM) output controlled by PREF1HI and PREF1LO.</td></tr>
<tr><td>PORTA7</td><td>200</td><td>I/O D5</td><td>General-purpose I/O port bit controlled by PADAT7 and PAEN7. This pin has one other possible function when PREF0EN=1.
When PREF0EN=1 and PAEN7=0, PORTA7 is a variable duty-cycle pulse reference generator (PWM) output controlled by PREF0HI and PREF0LO.</td></tr>
<tr><td>PORTB0</td><td>57</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT0 and PBEN0. PORTB0 can also function as GRO0 when in 48 bit graphics input mode; VR0 when in 24 bit RGB video input mode; Y0 when in 24 bit YUV video input mode.</td></tr>
<tr><td>PORTB1</td><td>58</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT1 and PBEN1. PORTB1 can also function as GRO1 when in 48 bit graphics input mode; VR1 when in 24 bit RGB video input mode; Y1 when in 24 bit YUV video input mode.</td></tr>
<tr><td>PORTB2</td><td>59</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT2 and PBEN2. PORTB2 can also function as:
<table><tr><th>Function</th><th>When in</th></tr><tr><td>DB1E</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DB0</td><td>30-bit output mode</td></tr><tr><td>GRO2</td><td>48-bit graphics input mode</td></tr><tr><td>VR2</td><td>24-bit RGB video input mode</td></tr><tr><td>Y2</td><td>24-bit YUV video input mode</td></tr><tr><td>Cb0</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
<tr><td>PORTB3</td><td>60</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT3 and PBEN3. PORTB3 can also function as:
<table><tr><th>Function</th><th>When in</th></tr><tr><td>DB1O</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DB1</td><td>30-bit output mode</td></tr><tr><td>GRO3</td><td>48-bit graphics input mode</td></tr><tr><td>VR3</td><td>24-bit RGB video input mode</td></tr><tr><td>Y3</td><td>24-bit YUV video input mode</td></tr><tr><td>Cb1</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
</table>

Table 2-6 Peripheral Interface Pin Descriptions (continued)

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>PORTB4</td><td>61</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT4 and PBEN4. PORTB4 can also function as:<table><tr><th>Function</th><th>When in</th></tr><tr><td>DG1E</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DG0</td><td>30-bit output mode</td></tr><tr><td>GRO4</td><td>48-bit graphics input mode</td></tr><tr><td>VR4</td><td>24-bit RGB video input mode</td></tr><tr><td>Y4</td><td>24-bit YUV video input mode</td></tr><tr><td>Y0</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
<tr><td>PORTB5</td><td>62</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT5 and PBEN5. PORTB5 can also function as:<table><tr><th>Function</th><th>When in</th></tr><tr><td>DG10</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DG1</td><td>30-bit output mode</td></tr><tr><td>GRO5</td><td>48-bit graphics input mode</td></tr><tr><td>VR5</td><td>24-bit RGB video input mode</td></tr><tr><td>Y5</td><td>24-bit YUV video input mode</td></tr><tr><td>Y1</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
<tr><td>PORTB6</td><td>63</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT6 and PBEN6. PORTB6 can also function as:<table><tr><th>Function</th><th>When in</th></tr><tr><td>DR1E</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DR0</td><td>30-bit output mode</td></tr><tr><td>GRO6</td><td>48-bit graphics input mode</td></tr><tr><td>VR6</td><td>24-bit RGB video input mode</td></tr><tr><td>Y6</td><td>24-bit YUV video input mode</td></tr><tr><td>Cr0</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
<tr><td>PORTB7</td><td>64</td><td>I/O D5</td><td>General purpose I/O port bit controlled by PBDAT7 and PBEN7. PORTB7 can also function as:<table><tr><th>Function</th><th>When in</th></tr><tr><td>DR1O</td><td>Dual-pixel 27-bit output mode</td></tr><tr><td>DR1</td><td>30-bit output mode</td></tr><tr><td>GRO7</td><td>48-bit graphics input mode</td></tr><tr><td>VR7</td><td>24-bit RGB video input mode</td></tr><tr><td>Y7</td><td>24-bit YUV video input mode</td></tr><tr><td>Cr1</td><td>30-bit YCbCr input mode (CSCD30BIT).</td></tr></table></td></tr>
</table>

Table 2-6 Peripheral Interface Pin Descriptions (continued)

Name	Pin(s)	Type	Function
PORTC0	39	I/O D5	General purpose I/O port controlled by PCDAT(7:0) and PCEN(7:0). PORTC(7:0) can also function as: Function / When GBO(7:0) / 48-bit graphics input mode VB(7:0) / 24-bit RGB video input mode U(7:0) / 24-bit YUV video input mode UV(7:0) / 16-bit YUV video input mode
PORTC1	40	I/O D5	
PORTC2	41	I/O D5	
PORTC3	42	I/O D5	
PORTC4	43	I/O D5	
PORTC5	44	I/O D5	
PORTC6	45	I/O D5	
PORTC7	46	I/O D5	
RXD	67	I/O U5	Serial Receive Data. RXD is the serial receive data for the on-chip serial port. This pin can also function as the 2-wire master data pin when 2WMEN=16.
TXD	68	I/O U5	Serial Transmit Data. TXD is the serial transmit data for the on-chip serial port. This pin can also function as the 2-wire master clock output pin when 2WMEN=16.

Table 2-7 provides detailed Miscellaneous pin descriptions.

Table 2-7 Miscellaneous Pin Descriptions

Name	Pin(s)	Type	Function
TESTEN	142	ID 5	Test Mode Enable. Connect to ground for normal operation.
RESET_N	139	BOD	Bidirectional reset pin. This pin requires a pull-up resistor to V33 (VDDQ3). The typical value is 3.3K ohm. • When EXTRSTEN=1, RESET_N is an input. • When EXTRSTEN=0, RESET_N is an output. In either case a low indicates reset.
EXTRSTEN	28	ID 5	External Reset Enable. • When EXTRSTEN=1, the internal reset is disabled and an external reset must be supplied on the RESET_N pin. • When EXTRSTEN=0, the internal reset is enabled and RESET_N becomes a bidirectional pin that can be used to either drive external logic in the system or receive an external reset signal.
XI	169	I	Crystal Input. Connect to external crystal. XI can also function as the MCLK input LVTTL-level signal from an external oscillator.
XO	170	O	Crystal Output. Connect to external crystal.

Table 2-8 provides detailed Microprocessor Debug Port pin descriptions.

Table 2-8 Microprocessor Debug Port Pin Descriptions

Name	Pin(s)	Type	Function
TRST_N	147	ID 5	Debug port reset (low true). Leave floating if debug port is not being used.
TCK	146	ID 5	Debug port serial data clock. Leave floating if debug port is not being used.
TMS	145	ID 5	Debug port mode select. Leave floating or pull to ground to disable.
TDI	144	ID 5	Debug port serial data in. Leave floating if debug port is not being used.
TDO	143	I/O D5	Debug port serial data out. Leave floating if debug port is not being used.

Table 2-9 provides detailed Power and Ground pin descriptions.

Table 2-9 Power and Ground Pin Descriptions

Name	Pin(s)	Type	Function
VDD1	16,37,65,84, 137,185	P	1.8V digital core power.
VSS	17,38,66,85, 138,186	P	Digital core ground.
VDDQ3	29,52,72,86, 104,123,140, 171,208	P	3.3V digital I/O power.
VSSQ	1, 30, 53, 73, 87, 105, 124, 141, 172,	P	Digital I/O ground.
VDDPA1	167	P	1.8V analog clock generator power.
VDDPA2	165	P	1.8V analog clock generator power.
VSSPA1	168	P	Clock generator analog ground.
VSSPA2	166	P	Clock generator analog ground.

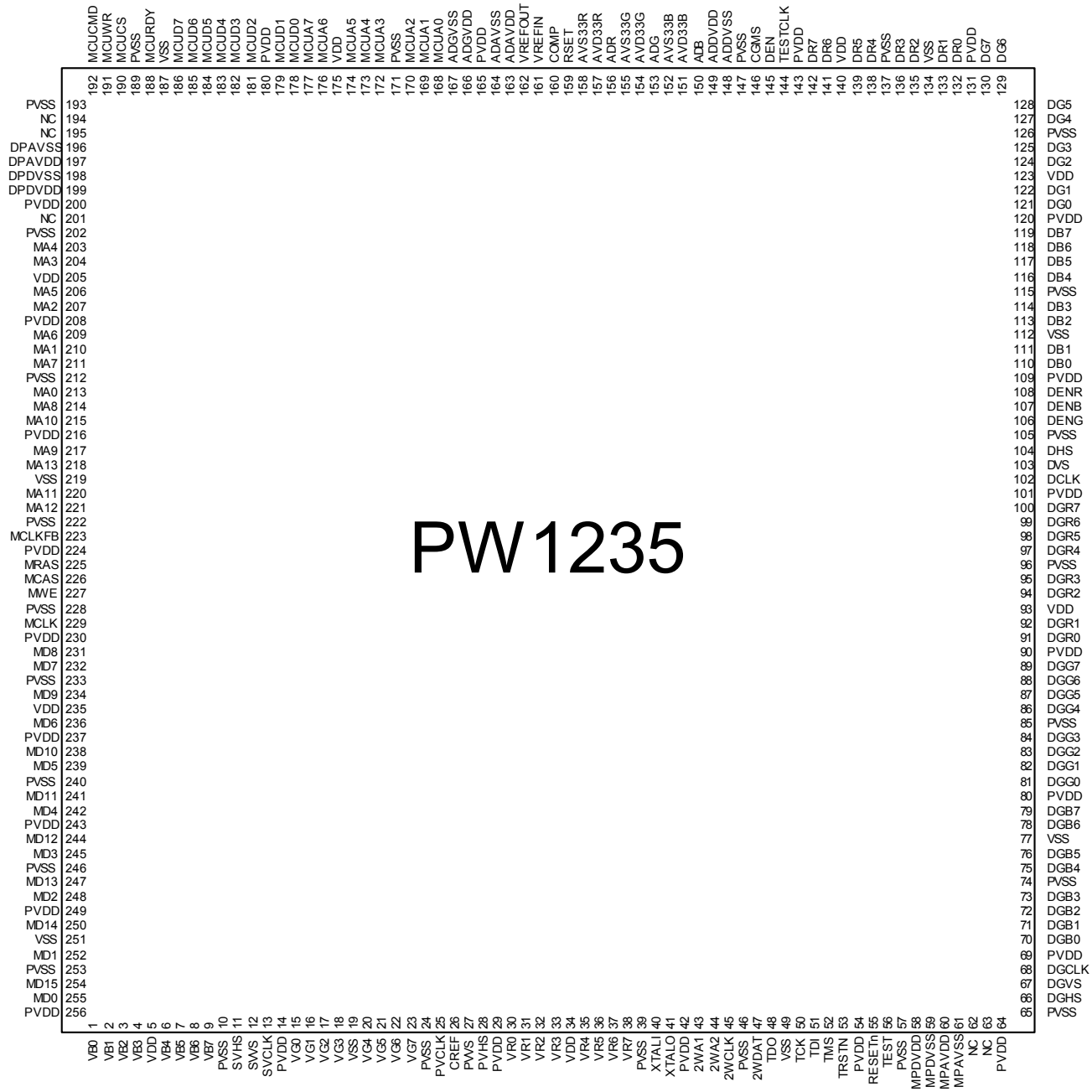


Figure 2-1 Pin Layout

2.2.1 Video Port Pins

Table 2-1 provides detailed pin descriptions for the Video Port.

Table 2-1 Video Port Pin Descriptions

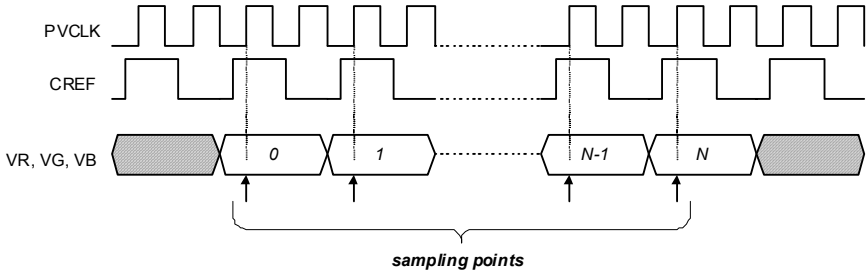
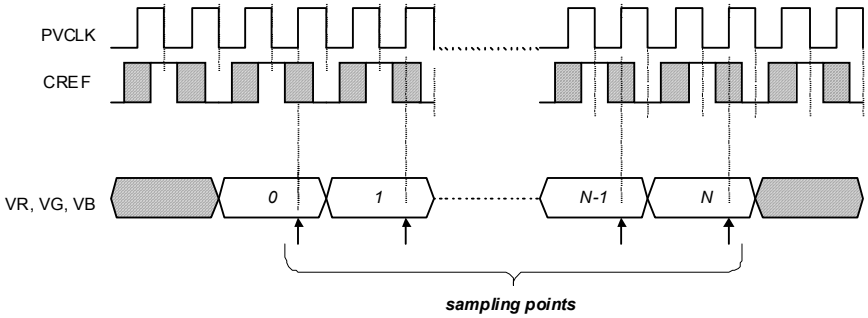
Name	Pin(s)	Type	Function
PVHS	28	I	Primary Video (PV) Port horizontal sync input. Indicates start of next line of input data. This signal is internally polarity corrected (PVHS_POL) so PVHS can be either active-high or active-low. [Input, pull-down, 5V-tolerant]
PVVS	27	I	Primary Video (PV) Port vertical sync input. Indicates start of next field or frame of input data. This signal is internally polarity corrected (PVVS_POL) so PVVS can be either active-high or active-low. [Input, pull-down, 5V-tolerant]
CREF	26	I	Video input clock reference. [Input, pull-down, 5V-tolerant] • cref_mode = 1  • cref_mode = 0 
PVCLK	25	I	Primary Video (PV) Port pixel clock input. [Input, pull-down, 5V-tolerant]
SVVS	12	I	Secondary Video (SV) Port (ITU-R BT656 format) vertical sync input. Indicates start of next field or frame of input data. This signal is internally polarity corrected (svvs_pol) so SVVS can be either active-high or active-low. [Input, pull-down, 5V-tolerant]
SVHS	11	I	Secondary Video (SV) Port (ITU-R BT656 format) horizontal sync input. This signal is internally polarity corrected (*svhs_pol*) so SVHS can be either active-high or active-low. [Input, pull-down, 5V-tolerant]
SVCLK	13	I	Secondary Video (SV) Port (ITU-R BT656 format) pixel clock input. [Input, pull-down, 5V-tolerant]

Table 2-1 Video Port Pin Descriptions (continued)

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>VR0</td><td>30</td><td>I</td><td rowspan="8">Video port red data input. These pins have different functions depending on the settings of the PVmode register. [Input, pull-down, 5V-tolerant]
<table><tr><th>PV_mode</th><th>VR[7:0] Pin Function</th></tr><tr><td>00</td><td>Reserved.</td></tr><tr><td>01</td><td>Primary Video (PV) Port.
UV[7:4]: ITU-R BT601 YUV 4:1:1 UV pixel data.</td></tr><tr><td>10</td><td>Primary Video (PV) Port
UV[7:0]: ITU-R BT601 YUV 4:2:2 UV pixel data.</td></tr><tr><td>11</td><td>Primary Video (PV) Port.
R[7:0]: red pixel data or
V[7:0]: ITU-R BT601 YUV 4:4:4 pixel data.</td></tr></table></td></tr>
<tr><td>VR1</td><td>31</td><td>I</td></tr>
<tr><td>VR2</td><td>32</td><td>I</td></tr>
<tr><td>VR3</td><td>33</td><td>I</td></tr>
<tr><td>VR4</td><td>35</td><td>I</td></tr>
<tr><td>VR5</td><td>36</td><td>I</td></tr>
<tr><td>VR6</td><td>37</td><td>I</td></tr>
<tr><td>VR7</td><td>38</td><td>I</td></tr>
<tr><td>VG0</td><td>15</td><td>I</td><td rowspan="8">Video port green data input. These pins have different functions depending on the settings of the Primary Video (PV) Port mode registers. [Input, pull-down, 5V-tolerant]
<table><tr><th>PV_mode</th><th>VG[7:0] Pin Function</th></tr><tr><td>00</td><td>Reserved.</td></tr><tr><td>01</td><td>Primary Video (PV) Port.
Y[7:0]: ITU-R BT601 YUV 4:1:1 UV pixel data.</td></tr><tr><td>10</td><td>Primary Video (PV) Port.
Y[7:0]: ITU-R BT601 YUV 4:2:2 UV pixel data.</td></tr><tr><td>11</td><td>Primary Video (PV) Port.
G[7:0]: green pixel data or
Y[7:0]: ITU-R BT601 YUV 4:4:4 pixel data.</td></tr></table></td></tr>
<tr><td>VG1</td><td>16</td><td>I</td></tr>
<tr><td>VG2</td><td>17</td><td>I</td></tr>
<tr><td>VG3</td><td>18</td><td>I</td></tr>
<tr><td>VG4</td><td>20</td><td>I</td></tr>
<tr><td>VG5</td><td>21</td><td>I</td></tr>
<tr><td>VG6</td><td>22</td><td>I</td></tr>
<tr><td>VG7</td><td>23</td><td>I</td></tr>
<tr><td>VB0</td><td>1</td><td>I</td><td rowspan="8">Video port blue data input. These pins have different functions depending on the settings for the Primary Video (PV) Port mode registers. [Input, pull-down, 5V-tolerant]
<table><tr><th>PV_mode</th><th>VB[7:0] Pin Function</th></tr><tr><td>00</td><td>Reserved.</td></tr><tr><td>01
10</td><td>Secondary Video (SV) Port
YUV[7:0]: ITU-R BT656 format pixel data.</td></tr><tr><td>11</td><td>Primary Video (PV) Port.
B[7:0]: blue pixel data or
U[7:0]: ITU-R BT601 YUV 4:4:4 pixel data.</td></tr></table></td></tr>
<tr><td>VB1</td><td>2</td><td>I</td></tr>
<tr><td>VB2</td><td>3</td><td>I</td></tr>
<tr><td>VB3</td><td>4</td><td>I</td></tr>
<tr><td>VB4</td><td>6</td><td>I</td></tr>
<tr><td>VB5</td><td>7</td><td>I</td></tr>
<tr><td>VB6</td><td>8</td><td>I</td></tr>
<tr><td>VB7</td><td>9</td><td>I</td></tr>
</table>

2.2.2 Digital/Graphics (DG) Port Pins

Table 2-2 provides detailed pin descriptions for the Digital/Graphics (DG) Port.

Table 2-2 Digital/Graphics (DG) Port Pin Descriptions

Name	Pin(s)	Type	Function
DGS	67	I	Digital/Graphics (DG) port vertical sync. [Tri-state output, 4mA drive, 5V-tolerant]
DGHS	66	I	Digital/Graphics (DG) port horizontal sync. [Tri-state output, 4mA drive, 5V-tolerant]
DGCLK	68	I	Digital/Graphics (DG) port pixel clock. [Tri-state output, 8mA drive, 5V-tolerant]

Table 2-2 Digital/Graphics (DG) Port Pin Descriptions (continued)

Name	Pin(s)	Type	Function
DGR0	91	I	Digital/Graphics (DG) port red data. [Bi-directional, input with pull-down, tri-state 4mA drive output, 5V-tolerant] **DGR[7:0] Pin Function** Digital/Graphics (DG) Port input (single pixel mode). R[7:0]: red pixel data or V[7:0]: YUV 4:4:4 pixel data.
DGR1	92	I	
DGR2	94	I	
DGR3	95	I	
DGR4	97	I	
DGR5	98	I	
DGR6	99	I	
DGR7	100	I	
DGG0	81	I	Digital/Graphics (DG) port green data. [Bi-directional, input with pull-down, tri-state 4mA drive output, 5V-tolerant] **DGG[7:0] Pin Function** Digital/Graphics (DG) Port input (single pixel mode). G[7:0]: green pixel data or Y[7:0]: YUV 4:4:4 pixel data.
DGG1	82	I	
DGG2	83	I	
DGG3	84	I	
DGG4	86	I	
DGG5	87	I	
DGG6	88	I	
DGG7	89	I	
DGB0	70	I	Digital/Graphics (DG) port blue data. [Bi-directional, input with pull-down, tri-state 4mA drive output, 5V-tolerant] **DGB[7:0] Pin Function** Digital/Graphics (DG) Port input (single pixel mode). B[7:0]: blue pixel data or U[7:0]: YUV 4:4:4 pixel data.
DGB1	71	I	
DGB2	72	I	
DGB3	73	I	
DGB4	75	I	
DGB5	76	I	
DGB6	78	I	
DGB7	79	I	

2.2.3 System Power Pins

Table 2-3 provides detailed pin descriptions for System Power.

Table 2-3 System Power Pin Descriptions

Name	Pin(s)	Type	Function
VDD	5, 34, 93, 123, 140, 175, 205, 235	P	Digital core power (2.5V).
VSS	19, 49, 77, 112, 134, 187, 219, 251	G	Digital core ground.

Table 2-3 System Power Pin Descriptions (continued)

Name	Pin(s)	Type	Function
PVDD	14, 29, 42, 54, 64, 69, 80, 90, 101, 109, 120, 131, 143, 165, 180, 200, 208, 216, 224, 230, 237, 243, 249, 256	P	Digital I/O power (3.3V).
PVSS	10, 24, 39, 46, 57, 65, 74, 85, 96, 105, 115, 126, 137, 147, 171, 189, 193, 202, 212, 222, 228, 233, 240, 246, 253	G	Ground.
MPAVDD	60	P	Memory PLL analog power 2.5V.
MPAVSS	61	G	Memory PLL analog ground.
MPDVDD	58	P	Memory PLL guard ring / digital power 2.5V.
MPDVSS	59	G	Memory PLL guard ring / digital ground.
DPAVDD	197	P	Display PLL analog power 2.5V.
DPAVSS	196	G	Display PLL analog ground.
DPDVDD	199	P	Display PLL digital power 2.5V.
DPDVSS	198	G	Display PLL digital ground.
AVD33R	157	P	Analog power (+3.3V) for R (V/Pr) channel.
AVD33G	154	P	Analog power (+3.3V) for G (Y/Y) channel.
AVD33B	151	P	Analog power (+3.3V) for B (U/Pb) channel.
AVS33R	158	G	Analog ground for R (V/Pr) channel.
AVS33G	155	G	Analog ground for G (Y/Y) channel.
AVS33B	152	G	Analog ground for B (U/Pb) channel.
ADAVDD	163	P	Analog power supply (+2.5V) for the analog display port.
ADAVSS	164	G	Analog ground for the analog display port.
ADDVDD	149	P	Digital power supply (+2.5V) for the analog display port.
ADDVSS	148	G	Digital ground for the analog display port.
ADGVDD	166	P	Guard ring power for the analog display port.
ADGVSS	167	G	Guard ring ground for the analog display port.

2.2.4 Miscellaneous Pins

Table 2-4 provides detailed descriptions for Miscellaneous Pins.

Table 2-4 Miscellaneous Pin Descriptions

Name	Pin(s)	Type	Function
XTALI	40	I	Crystal oscillator input. Connect to an external 10MHz crystal.
XTALO	41	O	Crystal oscillator output. Connect to an external 10MHz crystal.
RESETn	55	I	Hardware asynchronous reset. The signal is active low. Must be continuously asserted for a minimum of 100 µs after power-up to satisfy the SDRAM power-up requirement. [Input, Schmitt trigger, pull-up, 5V-tolerant]
CGMS	146	I	CGMS Enable
TCK	50	I	Debug port test data clock. TCK provides the clock input for the Test Bus (also known as the Test Access Port).
TDI	51	I	Debug port test data in. TDI transfers serial test data into VISTA. TDI provides the serial input necessary for JTAG specification support.
TDO	48	O	Debug port test data out. TDO transfers serial test data out of VISTA. TDO provides the serial input necessary for JTAG specification support.
TMS	52	I	Debug port test mode select. TMS is a JTAG specification support signal used by debug tools.
TRSTn	53	I	Debug port test reset. TRSTn resets the Test Access Port (TAP) logic. TRSTn must be driven low during power on RESETn.
TEST	56	I	Test mode. Active high. Must be low during normal operation. [Input, pull-down, 5V-tolerant]
TESTCLK	144	I	Used for testing, can be used to supply display clock. [Input, pull-down, 5V-tolerant]
NC	201	-	No connect.
NC	62, 63, 194,195	-	No connect.

2.2.5 Host Interface Pins

Table 2-5 provides detailed pin descriptions for the Host Interface.

Table 2-5 Host Interface Pin Descriptions

Name	Pin(s)	Type	Function
2WCLK	45	I	Clock signal of two-wire serial bus. [Input, pull-up, 5V-tolerant]
2WDAT	47	I/O	Data signal of two-wire serial bus. [Bi-directional, tri-state 4mA drive output, 5V-tolerant]
2WA1	43	I	Programmable two-wire serial bus address bit 1. [Input, pull-down, 5V-tolerant]
2WA2	44	I	Programmable two-wire serial bus address bit 2. [Input, pull-down, 5V-tolerant]

2.2.6 Memory Pins

Table 2-6 provides detailed pin descriptions for Memory.

Table 2-6 Memory Pin Descriptions

Name	Pin(s)	Type	Function
MCLK	229	O	SDRAM clock. This signal is rising edge active. [Tri-state output, 8mA drive, 5V-tolerant]
MCLKFB	223	I	SDRAM clock feedback. For latching in read data. [Input, 5V-tolerant]

Table 2-6 Memory Pin Descriptions (continued)

Name	Pin(s)	Type	Function
MRAS	225	O	SDRAM row address strobe. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
MCAS	226	O	SDRAM column address strobe. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
MWE	227	O	SDRAM write enable. This signal is active low. [Tri-state output, 8mA drive, 5V-tolerant]
MA0	213	O	SDRAM address bus. Multiplexed row and column address and bank select. Row addresses use MA[11:0] for 8MB SDRAM and MA[10:0] for 2MB SDRAM. Column addresses use MA[7:0]. [Tri-state output, 8mA drive, 5V-tolerant] ***Note***: MA10 is a control signal during column address charging and pre-charging. For 8MB SDRAM the bank select pins ba0 and ba1 should be connected to MA12 and MA13, respectively. For 2MB SDRAM, connect ba0 to MA12.
MA1	210	O	
MA2	207	O	
MA3	204	O	
MA4	203	O	
MA5	206	O	
MA6	209	O	
MA7	211	O	
MA8	214	O	
MA9	217	O	
MA10	215	O	
MA11	220	O	
MA12	221	O	
MA13	218	O	
MD0	255	I/O	SDRAM data bus. [Bi-directional, tri-state 8mA drive output, pull-up, 5V-tolerant]
MD1	252	I/O	
MD2	248	I/O	
MD3	245	I/O	
MD4	242	I/O	
MD5	239	I/O	
MD6	236	I/O	
MD7	232	I/O	
MD8	231	I/O	
MD9	234	I/O	
MD10	238	I/O	
MD11	241	I/O	
MD12	244	I/O	
MD13	247	I/O	
MD14	250	I/O	
MD15	254	I/O	

2.2.7 Digital Display Output Port Pins

Table 2-7 provides detailed pin descriptions for the Digital Display Output Port.

Table 2-7 Digital Display Output Port Pin Descriptions

Name	Pin(s)	Type	Function
DVS	103	O	Digital display output port vertical sync. [Tri-state output, 4mA drive, 5V-tolerant]
DHS	104	O	Digital display output port horizontal sync. [Tri-state output, 4mA drive, 5V-tolerant]
DCLK	102	O	Digital display output port pixel clock. [Tri-state output, 8mA drive, 5V-tolerant]

Table 2-7 Digital Display Output Port Pin Descriptions (continued)

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>DENR</td><td>108</td><td>O</td><td>Display pixel enable red. [Tri-state output, 4mA drive, 5V-tolerant]</td></tr>
<tr><td>DENG</td><td>106</td><td>O</td><td>Digital display pixel enable green. [Tri-state output, 4mA drive, 5V-tolerant]</td></tr>
<tr><td>DENB</td><td>107</td><td>O</td><td>Digital display pixel enable blue. [Tri-state output, 4mA drive, 5V-tolerant]</td></tr>
<tr><td>DEN</td><td>145</td><td>I</td><td>Digital display output port output enable. [Input, pull-up, 5V-tolerant]
Active level controlled by DEN_POL [reg 0x61 bit 2].
Note: DEN only controls the data bus [DR(7:0), DG(7:0), DB(7:0)] and not the control signals [DVS, DHS, DCLK, DENR, DENG, DENB].</td></tr>
<tr><td>DR0</td><td>132</td><td>O</td><td rowspan="8">Digital display output port red data. [Tri-state output, 4mA drive, 5V-tolerant]
<table>
<tr><th></th><th>uv_mode</th><th>DR[7:0] Pin Function</th></tr>
<tr><td rowspan="2"></td><td>000</td><td>DPort single pixel output.
R[7:0]: red pixel data or
V[7:0]: YUV 4:4:4 pixel data.</td></tr>
<tr><td>011</td><td>UV[7:0]: ITU-R BT601 YUV 4:2:2 pixel data</td></tr>
</table></td></tr>
<tr><td>DR1</td><td>133</td><td>O</td></tr>
<tr><td>DR2</td><td>135</td><td>O</td></tr>
<tr><td>DR3</td><td>136</td><td>O</td></tr>
<tr><td>DR4</td><td>138</td><td>O</td></tr>
<tr><td>DR5</td><td>139</td><td>O</td></tr>
<tr><td>DR6</td><td>141</td><td>O</td></tr>
<tr><td>DR7</td><td>142</td><td>O</td></tr>
<tr><td>DG0</td><td>121</td><td>O</td><td rowspan="8">Digital display output port green data. [Tri-state output, 4mA drive, 5V-tolerant]
<table>
<tr><th></th><th>uv_mode</th><th>DG[7:0] Pin Function</th></tr>
<tr><td rowspan="2"></td><td>000</td><td>DPort single pixel output.
G[7:0]: green pixel data or
Y[7:0]: YUV 4:4:4 pixel data</td></tr>
<tr><td>011</td><td>Y[7:0]: ITU-R BT601 YUV 4:2:2 pixel data</td></tr>
</table></td></tr>
<tr><td>DG1</td><td>122</td><td>O</td></tr>
<tr><td>DG2</td><td>124</td><td>O</td></tr>
<tr><td>DG3</td><td>125</td><td>O</td></tr>
<tr><td>DG4</td><td>127</td><td>O</td></tr>
<tr><td>DG5</td><td>128</td><td>O</td></tr>
<tr><td>DG6</td><td>129</td><td>O</td></tr>
<tr><td>DG7</td><td>130</td><td>O</td></tr>
<tr><td>DB0</td><td>110</td><td>O</td><td rowspan="8">Digital display output port blue data. [Tri-state output, 4mA drive, 5V-tolerant]
<table>
<tr><th></th><th>uv_mode</th><th>DB[7:0] Pin Function</th></tr>
<tr><td></td><td>xxx</td><td>DPort single pixel output.
B[7:0]: blue pixel data or
U[7:0]: YUV 4:4:4 pixel data.</td></tr>
</table></td></tr>
<tr><td>DB1</td><td>111</td><td>O</td></tr>
<tr><td>DB2</td><td>113</td><td>O</td></tr>
<tr><td>DB3</td><td>114</td><td>O</td></tr>
<tr><td>DB4</td><td>116</td><td>O</td></tr>
<tr><td>DB5</td><td>117</td><td>O</td></tr>
<tr><td>DB6</td><td>118</td><td>O</td></tr>
<tr><td>DB7</td><td>119</td><td>O</td></tr>
</table>

2.2.8 Analog Display Port Pins

Table 2-8 provides detailed pin descriptions for the Analog Display Port.

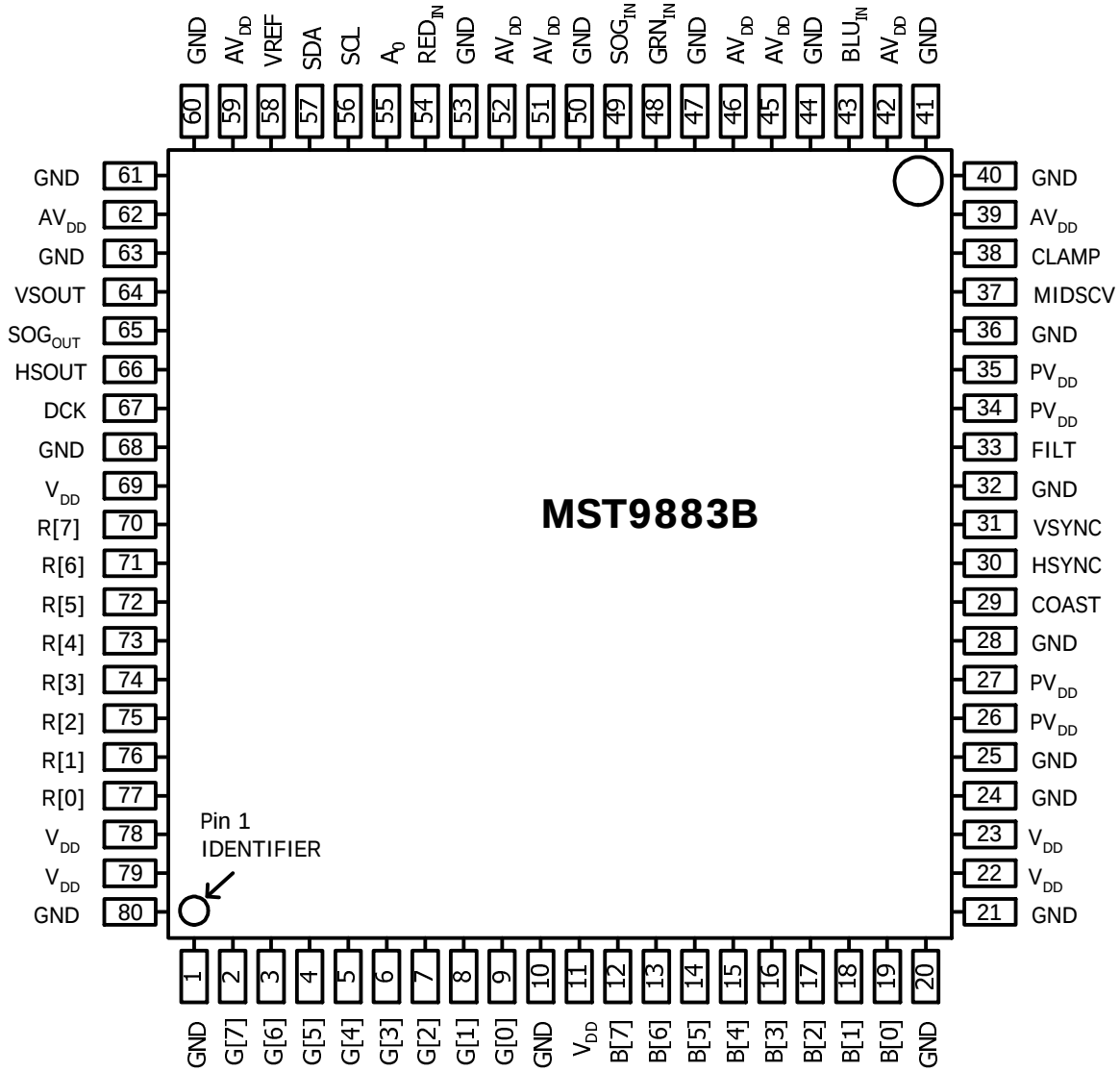
Table 2-8 Analog Display Port Pin Descriptions

Name	Pin(s)	Type	Function
ADR	156	O	Analog display port red (V/Pr) data.
ADG	153	O	Analog display port green (Y/Y) data.
ADB	150	O	Analog display port blue (U/Pb) data.
VREFIN	161	I	Reference voltage input.
VREFOUT	162	O	Voltage reference output. This output nominally delivers 1.23v reference voltage from bandgap reference block. It is normally connected to VREFIN pin.

Table 2-8 Analog Display Port Pin Descriptions (continued)

Name	Pin(s)	Type	Function
RSET	159	I/O	Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. RSET(ohm)=VREFIN(V)*10.66/IOFS(A), where IOFS is full-scale output current.
COMP	160	i/O	Compensation pin. This pin should be connected through 0.1uF ceramic capacitor to AVD33 (+3.3v) externally.

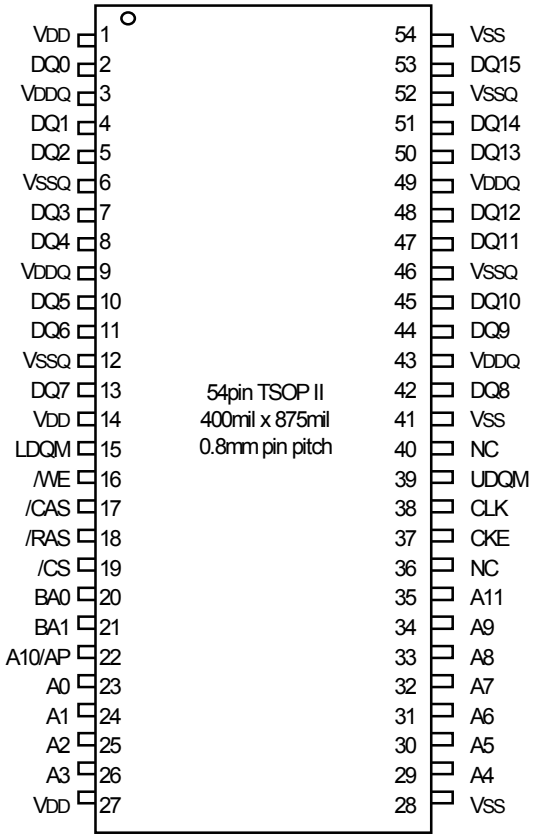
PIN CONFIGURATION



PIN DESCRIPTIONS

Pin Name	Pin Type	Function	Pin Number(s)
RED_{IN}	Analog Input	Red analog input	54
GRN_{IN}	Analog Input	Green analog input	48
BLU_{IN}	Analog Input	Blue analog input	43
SOG_{IN}	Analog Input	Sync on Green analog input	49
CLAMP	Digital CMOS Input	External Clamp Input	38
HSYNC	Digital CMOS Input	Horizontal SYNC Input	30
VSYNC	Digital CMOS Input	Vertical SYNC Input	31
COAST	Digital CMOS Input	Hold PLL Frequency, do not track HSYNC	29
SCL	Digital CMOS Input	Serial Interface clock	56
SDA	Digital CMOS Input/Output	Serial Interface data pin	57
A_0	Digital CMOS Input	Serial interface address pin	55
R [7:0]	Digital CMOS 3-state Output	Red output data	70-77
G [7:0]	Digital CMOS 3-state Output	Green output data	2-9
B [7:0]	Digital CMOS 3-state Output	Blue output data	12-19
DCK	Digital CMOS 3-state Output	Output data clock	67
HSOUT	Digital CMOS 3-state Output	HSYNC output	66
VSOUT	Digital CMOS 3-state Output	VSYNC output	64
SOG_{OUT}	Digital CMOS 3-state Output	SYNC on Green Slicer Output	65
FILT		No Connection	33
VREF	Reference	Internal Reference Bypass	58
MIDSCV	Reference	Internal Mid-Scale Voltage Bypass	37
AV_{DD}	3.3v Power	Analog Power	39,42,45,46,51,52,59,62
PV_{DD}	3.3v Power	PLL Power	26,27,34,35
V_{DD}	3.3v Power	Digital Output Power	11,22, 23, 69,78,79
GND	System Ground	System Ground	1,10,20,21,24,25,28,32,36,40,41,44,47,50,53,60,61,63,68,80

PIN CONFIGURATION

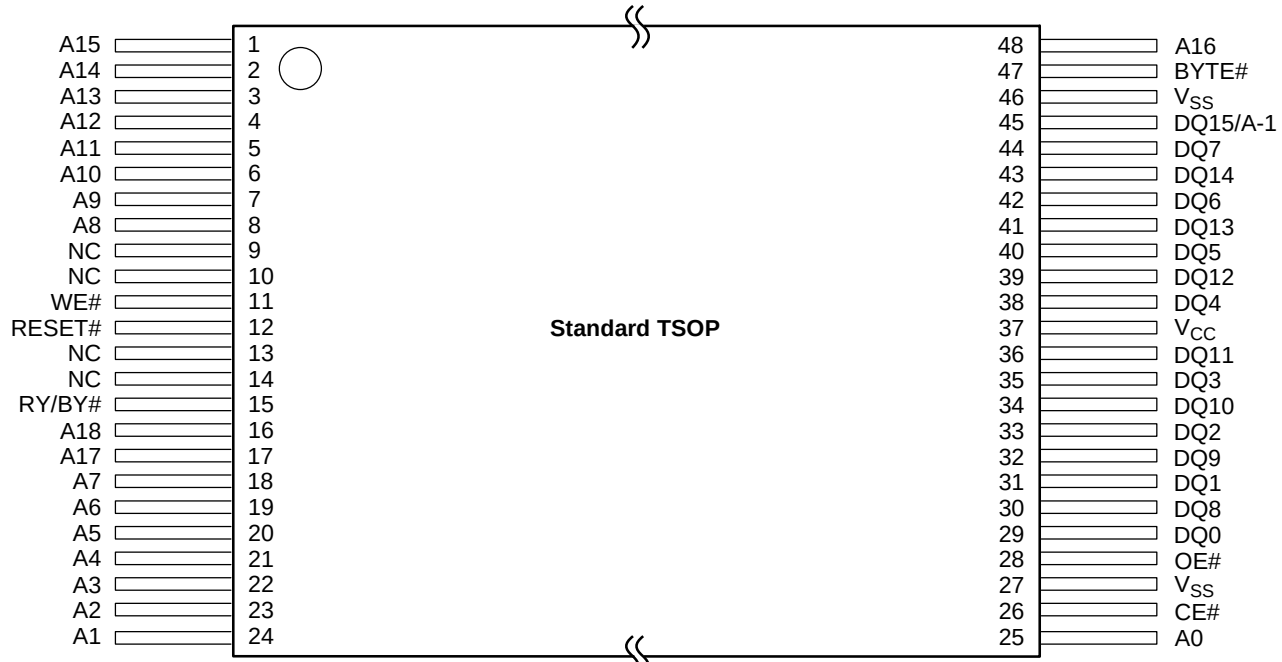


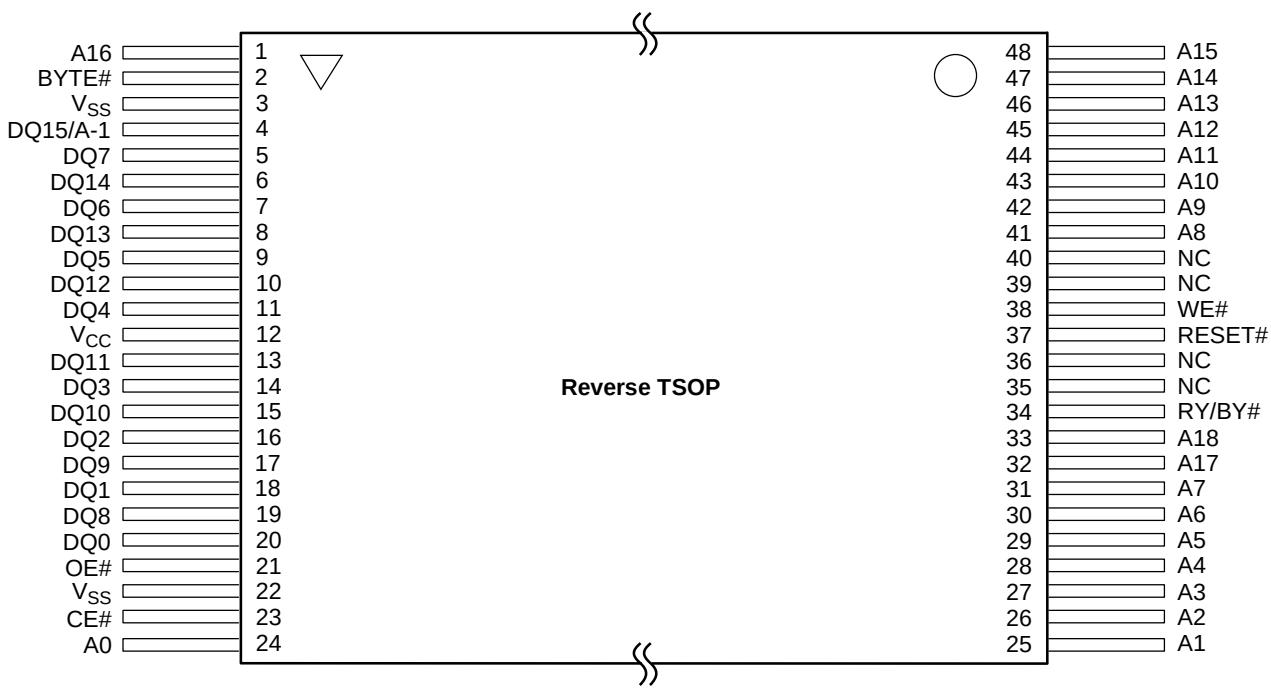
PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21536 for more information.

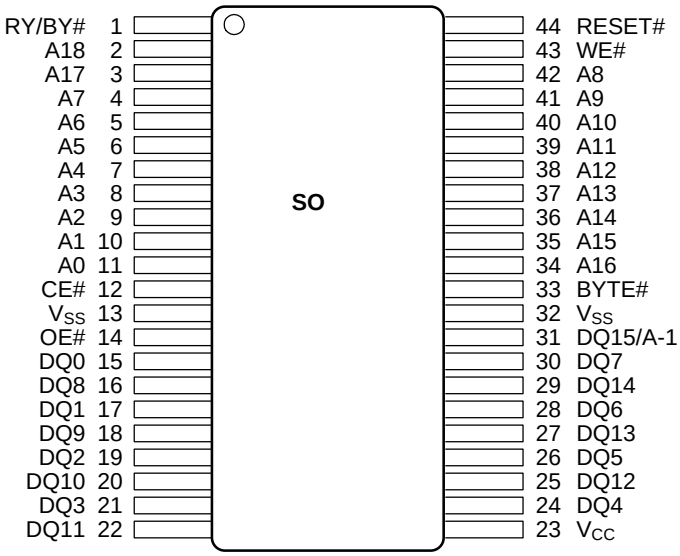




21490G-2

CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21536 for more information.



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	NC	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions for FBGA Package

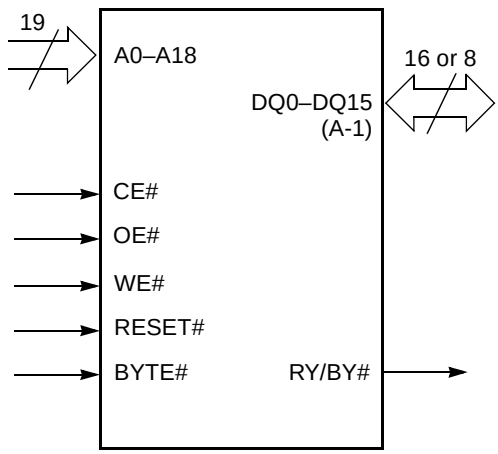
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A18	=	19 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy# output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



PIN DESCRIPTION

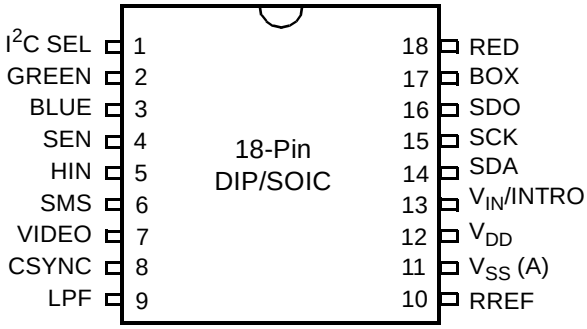


Figure 2. Z86229 Pin Configuration

Table 1. Z86229 Pin Identification*

No.	Symbol	Function	Direction
1	I^2C SEL	I^2C Address Selection	Input
2	GREEN	Video Output	Output
3	BLUE	Video Output	Output
4	SEN	Serial Enable	Input
5	HIN	Horizontal In	Input
6	SMS	Serial Mode Select	Input
7	VIDEO	Composite Video	Input
8	CSYNC	Composite Sync	Output
9	LPF	Loop Filter	Output
10	RREF	Resistor Reference	Input
11	V_{SS} (A)	Pwr. Supply (Analog) GND	
12	V_{DD}	Power Supply	
13	V_{IN}/INTRO	Vertical In/Interrupt Out	In/Output
14	SDA	Serial Data	In/Output
15	SCK	Serial Clock	Input
16	SDO	Serial Data Out	Output
17	BOX	OSD Timing Signal	Output
18	RED	Video Output	Output

Note: *DIP and SOIC pin configurations are identical.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to 6.0	V
V_{IN}	DC Input Voltage	–0.5 to V_{DD} +0.5	V
V_{OUT}	DC Output Voltage	–0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current per Pin	+10	mA
I_{OUT}	DC Output Current per Pin	+20	mA
I_{DD}	DC Supply Current	+30	mA
P_D	Power Dissipation per Device	300	mW
T_{STG}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

Notes:
*Voltages referenced to V_{SS} (A). Values beyond the maximum ratings listed above may cause damage to the device. Functional operation should be restricted to the limits specified in the DC and AC Characteristics tables or Pin Description section.

PIN DEFINITIONS

Inputs

I^2C SEL (Pin 1). This pin selects 28h for writing and 29h for reading when this input is Low(0). When the input is High(1), the device selects 2Ah for writing and 2Bh for reading.

SEN (Pin 4). This pin enables the signal for the SPI mode of operation on the Serial Control Port. When this pin is Low (0), the SPI port is disabled and the SDO pin is in the high-impedance state. Transitions on the SCK and SDA pins are ignored. SPI mode operation is enabled when SMS is High (1).

HIN (Pin 5). For this pin, the Horizontal Sync input signal at the CMOS level must be supplied. When the device is used in VIDEO-LOCK mode, the signal pulls the on-chip VCO within the proper range. The circuit uses the frequency of this signal, which must be within $\pm 3\%$ F_h, but the overall signal can be of either polarity. When used in the H-lock mode, the VCO phase locks to the rising edge of this signal. The HPOL bit of the H Position register can be set to operate with either polarity of input signal. This signal is usually the H Flyback signal. The timing difference between HIN rising edge and the leading edge of composite sync (of VIDEO input) is one of the factors which affects the horizontal position of the display. Any shift resulting from the timing of this signal can be compensated for with the horizontal timing value in the H Position Register. H-lock is intended for use when the part is generating an OSD display when no video signal is present.

SMS (Pin 6). This pin allows the mode select pin for the Serial Control Port. When this input is at a CMOS High state (1), the Serial Control Port operates in the SPI mode. When the input is Low (0), the Serial Control Port operates in the I^2C slave mode. In SPI mode, the SEN pin must be tied High. (See Reset Operation section.)

VIDEO (Pin 7). This pin is a composite NTSC video input, 1.0V p-p (nom), band limited to 600 kHz. The circuit operates with signal variation between 0.7–1.4V p-p. The polarity is sync tips negative. This signal pin should be AC coupled through a 0.1 µF capacitor, driven by a source impedance of 470 ohms or less.

SCK (Pin 15). This pin is an input for a serial clock signal from the master control device. In I^2C mode operation, the clock rate is expected to be within I^2C limits. In SPI mode, the maximum clock frequency is 10 MHz.

Reset Operation. When the SMS and SEN pins are both in the Low (0) state, the part is in the Reset state; therefore, in the I^2C mode, the SEN pin can be used as an NReset input. When SPI mode is used, if three wire operation is required, both SMS and SEN can be tied together and used as the NReset input. In either mode, NReset must be held Low (0) for at least 100 ns.

Input/Output

V_{IN}/INTRO (Pin 13). In external (EXT) vertical lock mode of operation, the internal vertical sync circuits lock to the V_{IN} input signal applied at this pin. The part locks to the rising or falling edge of the signal in accordance with the setting of the V Polarity command. The default is rising edge. The V_{IN} pulse must be at least 2 lines wide.

In INTRO Mode, when configured for internal vertical synchronization, this pin is an output pin providing an interrupt signal to the master control device in accordance with the settings in the Interrupt Mask Register.

SDA (Pin 14). When the Serial Control Port has been set to I^2C mode operation, this pin serves as the bidirectional data line for sending and receiving serial data. In SPI mode operation, the device operates as a serial data input. SPI mode output data is available on the SDO pin.

Outputs

RED, GREEN, BLUE (Pins 2, 3, 18). These pins are positive-acting CMOS-level signals.

- Color Mode: Red, Green, and Blue characters are incorporated as video outputs for use in a color receiver
- Mono Mode: In this mode, all three outputs carry the character luminance information

Note: The selection of Color/Mono Mode is user controlled in bit D_1 of the Configuration Register (Address=00h). (See Internal Registers section.)

CSync (Pin 8). Sync slice level. A 0.1 µF capacitor must be tied between this pin and analog ground V_{SS}(A). This capacitor stores the sync slice level voltage.

LPF (Pin 9). Loop Filter. A series RC low-pass filter must be tied between this pin and analog ground V_{SS}(A). There must also be second capacitor from the pin to V_{SS}(A).

PIN DEFINITIONS (Continued)

RREF (Pin 10). Reference setting resistor. Resistor must be 10 kOhms, ±2%.

SDO (Pin 16). This pin provides the serial data output when SPI mode communications have been selected. This pin is not used in I^2C mode operation.

BOX (Pin 17). Black box keying output is an active High, CMOS-level signal used to key in the black box for captions/text displays. This output is in a high-impedance state when the background attribute has been set to semi-transparent.

Power Supply

V_{SS} (Pins 11). These pins are the lowest potential power pins for the analog and digital circuits. They are normally tied to system ground.

V_{DD} (Pin 12). The voltage on this pin is nominally 5.0 Volts, and may range between 4.75 to 5.25 Volts with respect to the V_{SS} pins.

Note: The recommended printed circuit pattern for implementing the power connection and critical components is referenced in the Recommended Application Information section on page 49.

General Description

The MM74HC374 high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

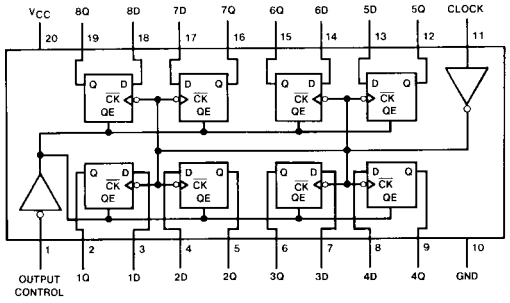
Ordering Code:

Order Number	Package Number	Package Description
MM74HC374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

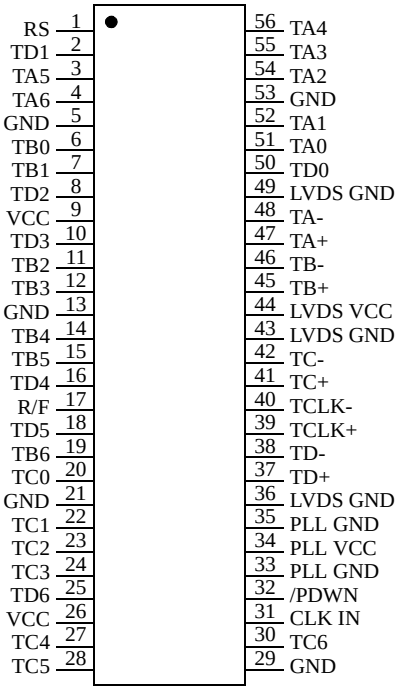
Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

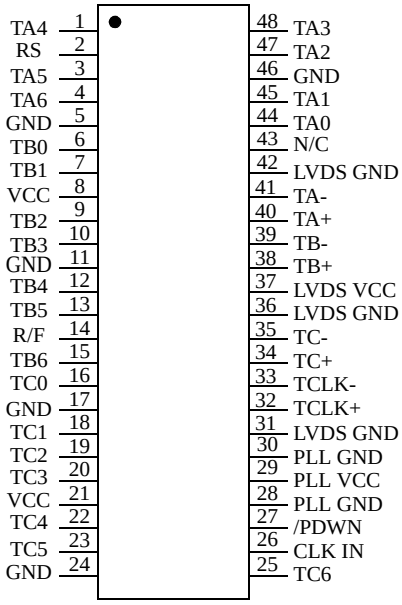
H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW-to-HIGH
Z = High Impedance State
Q_0 = The level of the output before steady state input conditions were established

Pin Out

THC63LVDM83R



THC63LVDM63R



THC63LVDM83R Pin Description

Pin Name	Pin #	Type	Description
TA+, TA-	47, 48	LVDS OUT	LVDS Data Out.
TB+, TB-	45, 46	LVDS OUT	
TC+, TC-	41, 42	LVDS OUT	
TD+, TD-	37, 38	LVDS OUT	
TCLK+, TCLK-	39, 40	LVDS OUT	LVDS Clock Out.
TA0 ~ TA6	51, 52, 54, 55, 56, 3, 4	IN	Pixel Data Inputs.
TB0 ~ TB6	6, 7, 11, 12, 14, 15, 19	IN	
TC0 ~ TC6	20, 22, 23, 24, 27, 28, 30	IN	
TD0 ~ TD6	50, 2, 8, 10, 16, 18, 25	IN	
/PDWN	32	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
RS	1	IN	LVDS swing control. RS: VCC → 350mV; : → :; GND → 200mV
R/F	17	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	9, 26	Power	Power Supply Pins for TTL inputs and digital circuitry.
CLKIN	31	IN	Clock in.
GND	5, 13, 21, 29, 53	Ground	Ground Pins for TTL inputs and digital circuitry.
LVDS VCC	44	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	36, 43, 49	Ground	Ground Pins for LVDS Outputs.
PLL VCC	34	Power	Power Supply Pin for PLL circuitry.
PLL GND	33, 35	Ground	Ground Pins for PLL circuitry.

THC63LVDM63R Pin Description

Pin Name	Pin #	Type	Description
TA+, TA-	40, 41	LVDS OUT	LVDS Data Out.
TB+, TB-	38, 39	LVDS OUT	
TC+, TC-	34, 35	LVDS OUT	
TCLK+, TCLK-	32, 33	LVDS OUT	LVDS Clock Out.
TA0 ~ TA6	44, 45, 47, 48, 1, 3, 4	IN	Pixel Data Inputs.
TB0 ~ TB6	6, 7, 9, 10, 12, 13, 15	IN	
TC0 ~ TC6	16, 18, 19, 20, 22, 23, 25	IN	
/PDWN	27	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
RS	2	IN	LVDS swing control. RS: VCC → 350mV; : → :; GND → 200mV

Pin Name	Pin #	Type	Description
R/F	14	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	8, 21	Power	Power Supply Pins for TTL inputs and digital circuitry.
CLKIN	26	IN	Clock in.
GND	5, 11, 17, 24, 46	Ground	Ground Pins for TTL inputs and digital circuitry.
LVDS VCC	37	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	36, 42	Ground	Ground Pins for LVDS Outputs.
PLL VCC	29	Power	Power Supply Pin for PLL circuitry.
PLL GND	28, 30	Ground	Ground Pins for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	continuous
Junction Temperature	+150°C
Storage Temperature Range	-65°C ~ +150°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation @+25°C	1.4W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	μA
I_{PD}	Pull Down Current	R/F pin, VIH=V_{CC}			100	μA
I_{RS}	RS Pull Down Current	RS pin, VIH=V_{CC}			100	μA

1. “Absolute Maximum Ratings” are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	–	–	–	–	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR data output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I^2S data output
6	12	10	5	4	I2S_WS	IN/OUT	LV	I^2S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I^2S clock
8	10	8	3	2	I2C_DA	IN/OUT	X	I^2C data
9	9	7	2	1	I2C_CL	IN/OUT	X	I^2C clock
10	8	–	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	X	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	X	I^2C Bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	–	76	59	NC		LV	Not connected
16	2	–	75	58	NC		LV	Not connected
17	–	–	–	–	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	53	TESTEN	IN	X	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF / LV	IF input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN–	IN	AVSS via 56 pF / LV	IF common (can be left vacant, only if IF input 1 is also not in use)

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	49	AVSUP		X	Analog power supply 5 V
–	–	–	65	–	AVSUP		X	Analog power supply 5 V
–	–	–	64	–	NC		LV	Not connected
–	–	–	63	–	NC		LV	Not connected
27	56	45	62	48	AVSS		X	Analog ground
–	–	–	61	–	AVSS		X	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
–	–	–	59	–	NC		LV	Not connected
29	54	43	58	46	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	–	55	43	ASG		AHVSS	Analog Shield Ground
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	–	52	40	ASG		AHVSS	Analog Shield Ground
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right
37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	–	49	37	ASG		AHVSS	Analog Shield Ground
39	44	–	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	–	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	–	–	46	–	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		X	Analog reference voltage
43	41	35	44	33	AHVSS		X	Analog ground
–	–	–	43	–	AHVSS		X	Analog ground
–	–	–	42	–	NC		LV	Not connected
–	–	–	41	–	NC		LV	Not connected
44	40	34	40	32	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		X	Analog power supply 8 V
46	38	32	38	30	CAPL_A		X	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF1		X	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	–	–	32	–	NC		LV	Not connected
53	32	–	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output
55	30	–	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		X	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
–	–	–	23	–	NC		LV	Not connected
–	–	–	22	–	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	X	Power-on-reset
62	23	–	20	15	NC		LV	Not connected
63	22	–	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I^2S2-data input
66	19	17	16	11	DVSS		X	Digital ground
–	–	–	15	–	DVSS		X	Digital ground
–	–	–	14	–	DVSS		X	Digital ground
67	18	16	13	10	DVSUP		X	Digital power supply 5 V
–	–	–	12	–	DVSUP		X	Digital power supply 5 V
–	–	–	11	–	DVSUP		X	Digital power supply 5 V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

4.3. Pin Descriptions

Pin numbers refer to the PQFP80 package.

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – I^2C Clock Input/Output (Fig. 4–18)
Via this pin, the I^2C-bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

Pin 3, **I2C_DA** – I^2C Data Input/Output (Fig. 4–18)
Via this pin, the I^2C-bus data is written to or read from the MSP.

Pin 4, **I2S_CL** – I^2S Clock Input/Output (Fig. 4–19)
Clock line for the I^2S bus. In master mode, this line is driven by the MSP; in slave mode, an external I^2S clock has to be supplied.

Pin 5, **I2S_WS** – I^2S Word Strobe Input/Output (Fig. 4–19)
Word strobe line for the I^2S bus. In master mode, this line is driven by the MSP; in slave mode, an external I^2S word strobe has to be supplied.

Pin 6, **I2S_DA_OUT** – I^2S Data Output (Fig. 4–23)
Output of digital serial sound data of the MSP on the I^2S bus.

Pin 7, **I2S_DA_IN1** – I^2S Data Input 1 (Fig. 4–15)
First input of digital serial sound data to the MSP via the I^2S bus.

Pin 8, **ADR_DA** – ADR Bus Data Output (Fig. 4–23)
Output of digital serial data to the DRP 3510A via the ADR bus.

Pin 9, **ADR_WS** – ADR Bus Word Strobe Output (Fig. 4–23)
Word strobe output for the ADR bus.

Pin 10, **ADR_CL** – ADR Bus Clock Output (Fig. 4–23)
Clock line for the ADR bus.

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a +5 V power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP.

Pin 17, **I2S_DA_IN2** – I^2S Data Input 2 (Fig. 4–15)
Second input of digital serial sound data to the MSP via the I^2S bus.

Pins 18, 19, 20, **NC** – Pins not connected.

Pin 21, **RESETQ** – Reset Input (Fig. 4–11)
In the steady state, high level is required. A low level resets the MSP 34x0G.

Pins 22, 23, **NC** – Pins not connected.

Pins 24, 25, **DACA_R/L** – Headphone Outputs (Fig. 4–21)
Output of the headphone signal. A 1-nF capacitor t AHVSS must be connected to these pins. The DC off set on these pins depends on the selected headphon volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connecte separately to ground (AHVSS). VREF2 serves as clean ground and should be used as the reference fo analog connections to the loudspeaker and head phone outputs.

Pins 27, 28, **DACM_R/L** – Loudspeaker Outputs (Fig. 4–21)
Output of the loudspeaker signal. A 1-nF capacitor t AHVSS must be connected to these pins. The DC off set on these pins depends on the selected loud speaker volume.

Pin 29, **NC** – Pin not connected.

Pin 30, **DACM_SUB** – Subwoofer Output (Fig. 4–21)
Output of the subwoofer signal. A 1-nF capacitor t AHVSS must be connected to this pin. Due to the lo frequency content of the subwoofer output, the valu of the capacitor may be increased for better suppres sion of high-frequency noise. The DC offset on this pi depends on the selected loudspeaker volume.

Pins 31, 32, **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–22)
Output of the SCART2 signal. Connections to thes pins must use a 100-Ω series resistor and are intende to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connecte separately to ground (AHVSS). VREF1 serves as clean ground and should be used as the reference fo analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–22)
Output of the SCART1 signal. Connections to thes pins must use a 100-Ω series resistor and are intende to be AC-coupled.

Pin 38, **CAPL_A** – Volume Capacitor Headphone (Fig. 4–24)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for headphone volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply.

Pin 40, **CAPL_M** – Volume Capacitor Loudspeaker (Fig. 4–24)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for loudspeaker volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Ground for Analog Power Supply High Voltage
Ground connection for the analog circuitry of the MSP (except IF input).

Pin 45, **AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3-µF and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs (Fig. 4–14)
The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pin 49, **ASG** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs (Fig. 4–14)
The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pin 52, **ASG** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 53, 54, **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–14)
The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pin 55, **ASG** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 56, 57, **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–14)
The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **VREFTOP** – Reference Voltage IF A/D Converter (Fig. 4–16)
Via this pin, the reference voltage for the IF A/D converter is decoupled. It must be connected to AVSS pins with a 10-µF and a 100-nF capacitor in parallel. Traces must be kept short.

Pin 59, **NC** – Pin not connected.

Pin 60, **MONO_IN** – Mono Input (Fig. 4–14)
The analog mono input signal is fed to this pin. Analog input connection must be AC-coupled.

Pins 61, 62, **AVSS*** – Ground for Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MSP.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

Pin 67, **ANA_IN1+** – IF Input 1 (Fig. 4–16)
The analog sound IF signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 68, **ANA_IN–** – IF Common (Fig. 4–16)
This pins serves as a common reference for ANA_IN1/2+ inputs.

Pin 69, **ANA_IN2+** – IF Input 2 (Fig. 4–16)
The analog sound if signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN2+ is internally connected to one input of a symmetrical op amp, ANA_IN– to the other.

Pin 70, **TESTEN** – Test Enable Pin (Fig. 4–12)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72, **XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–20)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL_IN. The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin enables factory test modes. For normal operation, it must be left vacant.

Pin 74, **AUD_CL_OUT** – Audio Clock Output (Fig. 4–20)
This is the 18.432 MHz main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, **D_CTR_I/O_1/0** – Digital Control Input/ Output Pins (Fig. 4–19)
General purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

Pin 79, **ADR_SEL** – I^2C Bus Address Select (Fig. 4–17)
By means of this pin, one of three device addresses for the MSP can be selected. The pin can be connected to ground (I^2C device addresses $80/81_{hex}$), to +5 V supply ($84/85_{hex}$), or left open ($88/89_{hex}$).

Pin 80, **STANDBYQ** – Stand-by
In normal operation, this pin must be high. If the MSP 34x0G is switched off by first pulling STANDBYQ low and then (after >1µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP (**'Standby'-mode**), the SCART switches maintain their position and function.

*** Application Note:**
All ground pins should be connected to one low-resistive ground plane. All supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with the lowest value should be placed nearest to the DVSUP and DVSS pins.

The ASG pins should be connected as closely as possible to the MSP ground. If they are lead with the SCART-inputs as shielding lines, they should not be connected to ground at the SCART connector.

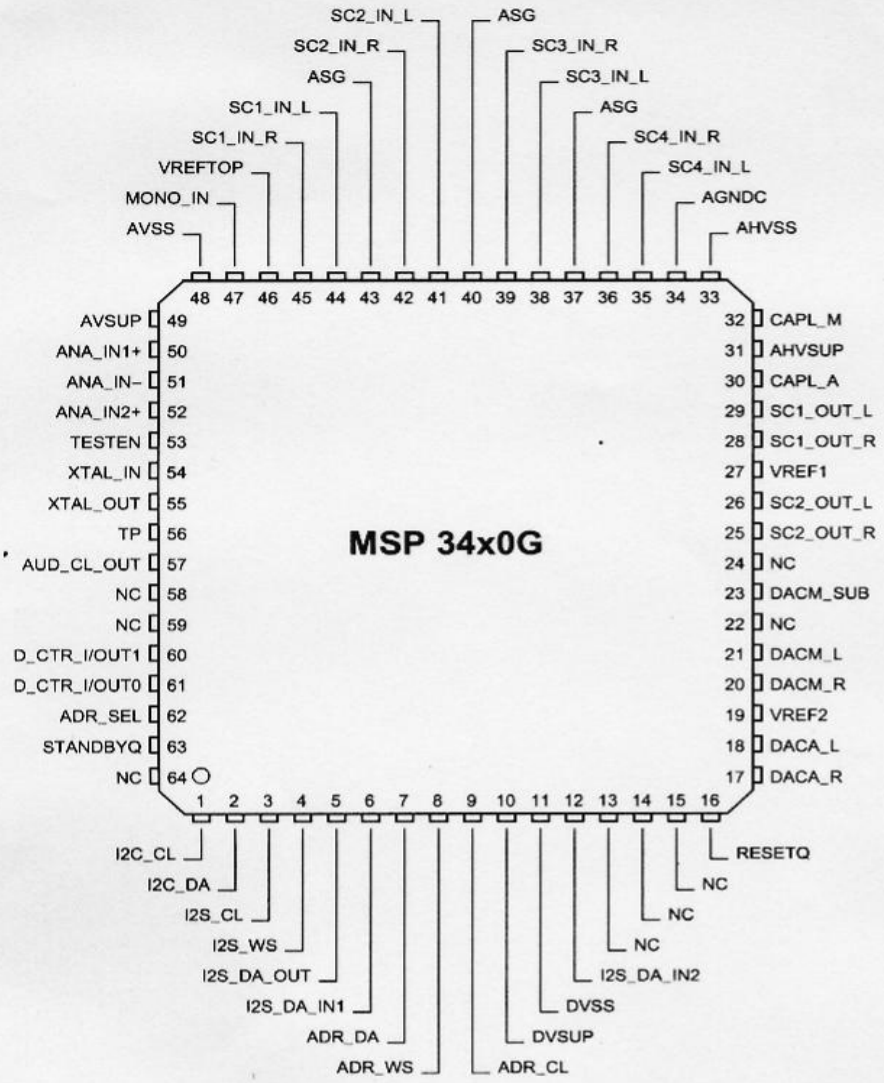


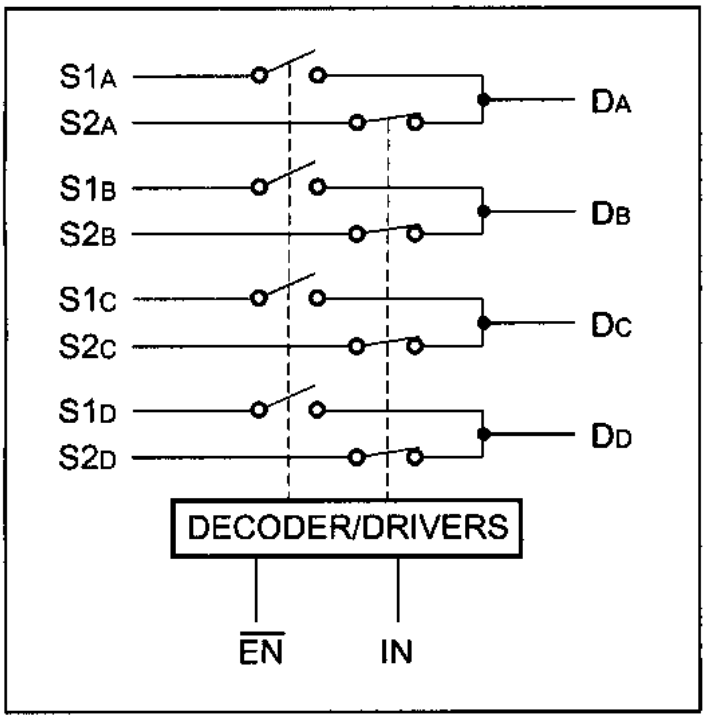
Fig. 4–10: PLQFP64 package

Low ON-Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: –58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

$\overline{EN}$	IN	ON Switch
0	0	S1A, S1B, S1C, S1D
0	1	S2A, S2B, S2C, S2D
1	X	Disabled

Product Description:

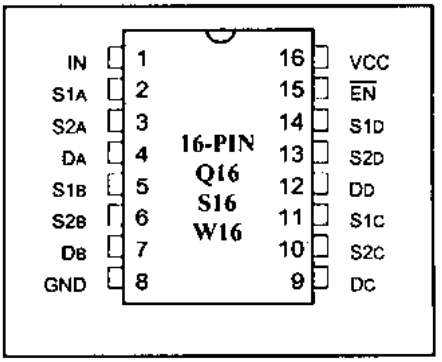
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
S1A, S2A S1B, S2B S1C, S2C S1D, S2D	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
DA, DB, DC, DD	Analog Video I/O
GND	Ground
VCC	Power

Pinning information

Pinning

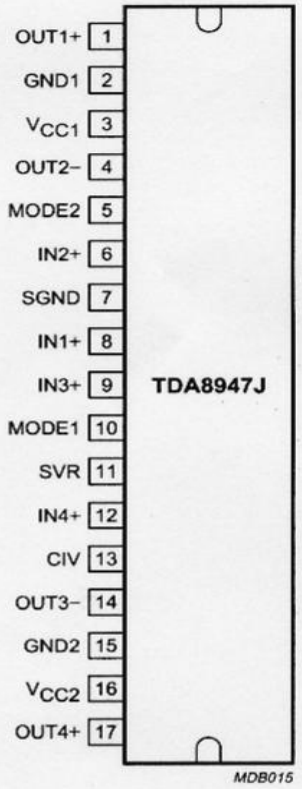


Fig 2. Pin configuration.

Pin description

Table 3: Pin description

Symbol	Pin	Description
OUT1+	1	non inverted loudspeaker output of channel 1
GND1	2	ground of channels 1 and 2
V_{CC1}	3	supply voltage channels 1 and 2
OUT2−	4	inverted loudspeaker output of channel 2
MODE2	5	mode selection 2 input: mute and on for channels 3 and 4
IN2+	6	input channel 2
SGND	7	signal ground
IN1+	8	input channel 1
IN3+	9	input channel 3
MODE1	10	mode selection 1 input: standby, mute and on for all channels
SVR	11	half supply voltage decoupling (ripple rejection)
IN4+	12	input channel 4

Symbol	Pin	Description
CIV	13	common input voltage decoupling
OUT3–	14	inverted loudspeaker output of channel 3
GND2	15	ground of channels 3 and 4
V_{CC2}	16	supply voltage channels 3 and 4
OUT4+	17	non inverted loudspeaker output of channel 4
TAB	-	back side tab or heats spreader has to be connected to ground

Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)}$$

For SE application R_i = 60 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \times 10^{3} \times 220 \times 10^{-9})} = 12 \text{ Hz}$$

For BTL application R_i = 30 kΩ and C_i = 470 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(30 \times 10^{3} \times 470 \times 10^{-9})} = 11 \text{ Hz}$$

As shown in Equation 2 and Equation 3, large capacitor values for the inputs are not necessary, so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

Power amplifier

The power amplifier is a BTL and/or SE amplifier with an all-NPN output stage, capable of delivering a peak output current of 4 A.

Using the TDA8947J as a BTL amplifier offers the following advantages:

- Low peak value of the supply current
- Ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance.

Specifications

Outline Dimensions

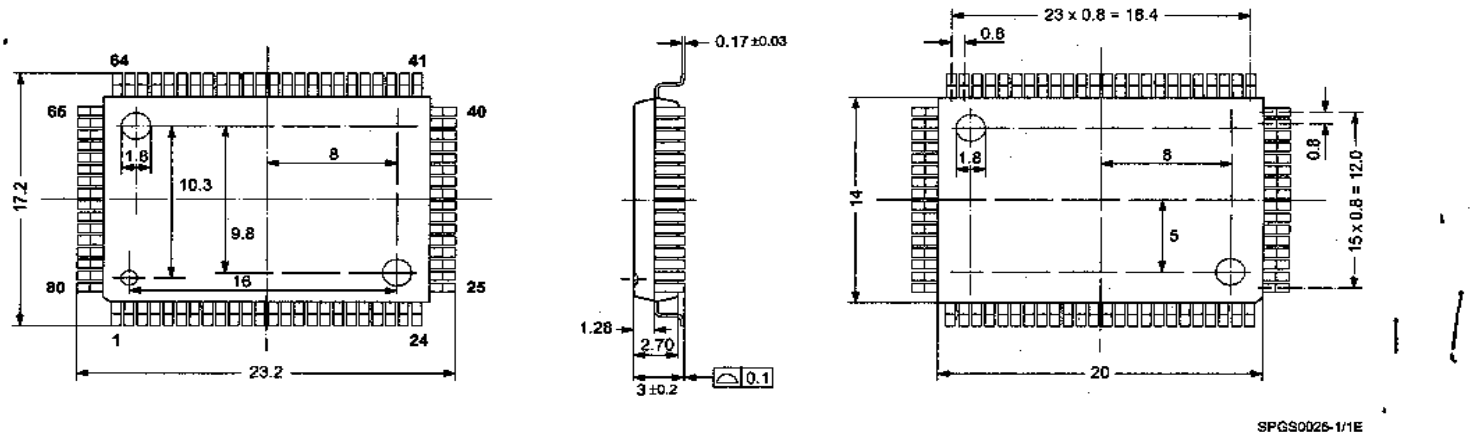


Fig. 4–1: 80-Pin Plastic Quad Flat Package **(PQFP80)**
Weight approximately 1.61 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA=4.75...5.25V, SUPPLYD=3.15...3.45V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input
3	R1/CR1IN	IN	VREF	Red1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Red2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
9	V_{SUPCAP}	SUPPLYD	X	Supply Voltage, Digital Decoupling Circuitry
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	SUPPLYD	X	Ground, Digital Decoupling Circuitry
13	SCL	IN/OUT	X	I^2C Bus Clock
14	SDA	IN/OUT	X	I^2C Bus Data

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	V_{SUPD}	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock Output 20.25 MHz
25	GND_{PA}	SUPPLYD	X	Ground, Pad Decoupling Circuitry
26	V_{SUPPA}	SUPPLYD	X	Supply Voltage, Pad Decoupling Circuitry
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground, Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC	OUT	LV	Front Sync/ Horizontal Clamp Pulse
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT	IN/OUT	LV	Front-End/Back-End Data
59	V_{STBY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog
67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV*	Chroma / Analog Video 5 Input
72	VIN1	IN	VRT*	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}
8, 61	NC	–	LV OR GND_D	Not connected

*) chroma selector must be set to 1 (CIN chroma select)

4.3. Pin Descriptions (pin numbers for PQFP80 package)

Pins 1-3 – Analog Component Inputs RGB1/YC_rC_b1 (Fig. 4–11)
These are analog component inputs with fast blank control. A RGB or YC_rC_b signal is converted using the component AD converter. The input signals must be AC-coupled.

Pins 4-6 – Analog Component Inputs RGB2/YC_rC_b2 (Fig. 4–11)
These are analog component inputs without fastblank control. A RGB or YC_rC_b signal is converted using the component AD converter. The input signals must be AC-coupled.

Pin 7, 64 – Ground, Analog Shield Front-End GND_F

Pin 9 – Supply Voltage, Decoupling Circuitry V_{SUPCAP}
This pin is connected with 220 nF/1.5 nF/390 pF to GND_{CAP}.

Pin 10 – Supply Voltage, Digital Circuitry V_{SUPD}

Pin 11 – Ground, Digital Circuitry GND_D

Pin 12 – Ground, Decoupling Circuitry GND_{CAP}

Pin 13– I^2C Bus Clock SCL (Fig. 4–3)
This pin connects to the I^2C bus clock line.

Pin 14– I^2C Bus Data SDA (Fig. 4–12)
This pin connects to the I^2C bus data line.

Pin 15 – Reset Input RESQ (Fig. 4–3)
A low level on this pin resets the VPC 32xx.

Pin 16 – Test Input TEST (Fig. 4–3)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pin 17 – VGAV-Input (Fig. 4–3)
This pin is connected to the vertical sync signal of a VGA signal.

Pin 18 – YC Output Enable Input YCOEQ (Fig. 4–3)
A low level on this pin enables the luma and chroma outputs.

Pin 19 – FIFO Input Enable FFIE (Fig. 4–4)
This pin is connected to the IE pin of the external field memory.

Pin 20 – FIFO Write Enable FFWE (Fig. 4–4)
This pin is connected to the WE pin of the external field memory.

Pin 21 – FIFO Reset Write/Read FFRSTW (Fig. 4–4)
This pin is connected to the RSTW pin of the external field memory.

Pin 22 – FIFO Read Enable FFRE (Fig. 4–4)
This pin is connected to the RE pin of the external field memory.

Pin 23 – FIFO Output Enable FFOE (Fig. 4–4)
This pin is connected to the OE pin of the external field memory.

Pin 24 – Main Clock Output CLK20 (Fig. 4–4)
This is the 20.25 MHz main clock output.

Pin 25 – Ground, Analog Pad Circuitry GND_{PA}

Pin 26 – Supply Voltage, Analog Pad Circuitry V_{SUPPA}
This pin is connected with 47 nF/1.5 nF to GND_{PA}

Pin 27 – Double Output Clock, LLC2 (Fig. 4–4)

Pin 28 – Output Clock, LLC1 (Fig. 4–4)
This is the clock reference for the luma, chroma, and status outputs.

Pin 29 – Supply Voltage, LLC Circuitry V_{SUPLLC}
This pin is connected with 68 nF to GND_{LLC}

Pin 30 – Ground, LLC Circuitry GND_{LLC}

Pins 31 to 34,37 to 40 – Luma Outputs Y7 – Y0 (Fig. 4–4)
These output pins carry the digital luminance data. The outputs are clocked with the LLC1 clock. In ITUR656 mode the Y/C data is multiplexed and clocked with LLC2 clock.

Pin 35– Ground, Luma Output Circuitry GND_Y
This pin is connected with 68 nF to GND_Y

Pin 36 – Supply Voltage, Luma Output Circuitry V_{SUPY}

Pins 41 to 44,47 to 50 – Chroma Outputs C7–C0 (Fig. 4–4) These outputs carry the digital CrCb chrominance data. The outputs are clocked with the LL1 clock. The CrCb data is sampled at half the clock rate and multiplexed. The CrCb multiplex is reset for each TV line. In ITUR656 mode, the chroma outputs are tri-stated.

Pin 45 – Supply Voltage, Chroma Output Circuitry V_{SUPC}
This pin is connected with 68 nF to GND_C

Pin 46 – Ground, Chroma Output Circuitry GND_C

Pin 51 – Ground, Sync Pad Circuitry GND_{SY}

Pin 52 – Supply Voltage, Sync Pad Circuitry V_{SUPSY}
This pin is connected with 47 nF/1.5 nF to GND_{SY}

Pin 53 – Interlace Output, INTLC (Fig. 4–4)
This pin supplies the interlace information, 0 indicates first field, 1 indicates second field.

Pin 54 – Active Video Output, AVO (Fig. 4–4)
This pin indicates the active video output data. The signal is clocked with the LLC1 clock.

Pin 55 – Front Sync/Horizontal Clamp Pulse, FSY/HC (Fig. 4 4)
This signal can be used to clamp an external video signal, that is synchronous to the input signal. The timing is programmable. In DIGIT3000 mode. this pin supplies the front sync information.

Pin 56 – Main Sync/Horizontal Sync Pulse MSY/HS (Fig. 4–4)
This pin supplies the horizontal sync pulse information in line-locked mode. In DIGIT3000 mode, this pin is the main sync input.

Pin 57 – Vertical Sync Pulse, VS (Fig. 4–4)
This pin supplies the vertical sync signal.

Pin 58 – Front-End/Back-End Data FPDAT (Fig. 4–5)
This pin interfaces to the DDP 3300A back-end processor. The information for the deflection drives and for the white drive control, i. e. the beam current limiter, is transmitted by this pin.

Pin 59 – Standby Supply Voltage V_{STDBY}
In standby mode, only the clock oscillator is active, GND_F should be ground reference. Please activate RESQ before powering-up other supplies

Pin 60 – CCU 5 MHz Clock Output CLK5 (Fig. 4–10)
This pin provides a clock frequency for the TV microcontroller, e.g. a CCU 3000 controller. It is also used by the DDP 3300A display controller as a standby clock.

Pins 62and 63 – XTAL1 Crystal Input and XTAL2 Crystal Output (Fig. 4–7)
These pins are connected to an 20.25 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. The CLK20 and CLK5 clock signals are derived from this oscillator. An external clock can be fed into XTAL1. In this case, clock frequency adjustment must be switched off.

Pin 65 – Ground, Analog Front-End GND_F

Pin 66 – Reference Voltage Top VRT (Fig. 4–8)
Via this pin, the reference voltage for the A/D converters is decoupled. The pin is connected with 10 µF/47 nF to the Signal Ground Pin.

Pin 67 I^2C Bus address select I2CSEL
This pin determines the I^2C bus address of the IC.

Table 4–1: VPC32xxD I^2C address select

I2CSEL	**I^2C Add.**
GND_F	88/89 hex
VRT	8C/8D hex
V_{SUPF}	8E/8F hex

Pin 68 – Signal GND for Analog Input ISGND (Fig. 4–10) This is the high quality ground reference for the video input signals.

Pin 69 – Supply Voltage, Analog Front-End V_{SUPF} (Fig. 4–8)
This pin is connected with 220 nF/1.5 nF/390 pF to GND_F

Pin 70 – Analog Video Output, VOUT (Fig. 4–6)
The analog video signal that is selected for the main (luma, CVBS) ADC is output at this pin. An emitter follower is required at this pin.

Pin 71 – Chroma Input CIN (Fig. 4–9)
This pin is connected to the S-VHS chroma signal. A resistive divider is used to bias the input signal to the

middle of the converter input range. CIN can only be connected to the chroma (Video 2) A/D converter. The signal must be AC-coupled.

Pins 72-75 – Video Input 1–4 (Fig. 4–11)
These are the analog video inputs. A CVBS or S-VHS luma signal is converted using the luma (Video 1) AD converter. The VIN1 input can also be switched to the chroma (Video 2) ADC. The input signal must be AC-coupled.

Pin 76 – Supply Voltage, Analog Component Inputs Front-End V_{SUPAI}
This pin is connected with 220 nF/1.5 nF/390 pF to GND_{AI}

Pin 77 – Ground, Analog Component Inputs Front-End GND_{AI}

Pin 78 – Reference Voltage Top VREF (Fig. 4–8)
Via this pin, the reference voltage for the analog component A/D converters is decoupled. The pin is connected with 10 µF/47 nF to the Analog Component Signal Ground Pin.

Pin 79 – Fast Blank Input FB1IN (Fig. 4–10)
This pin is connected to the analog fast blank signal. It controls the insertion of the RGB1/YC_rC_b1 signals. The input signal must be DC-coupled.

Pin 80 – Signal GND for Analog Component Inputs AISGND (Fig. 4–10)
This is the high quality ground reference for the component input signals.

Pin Configuration

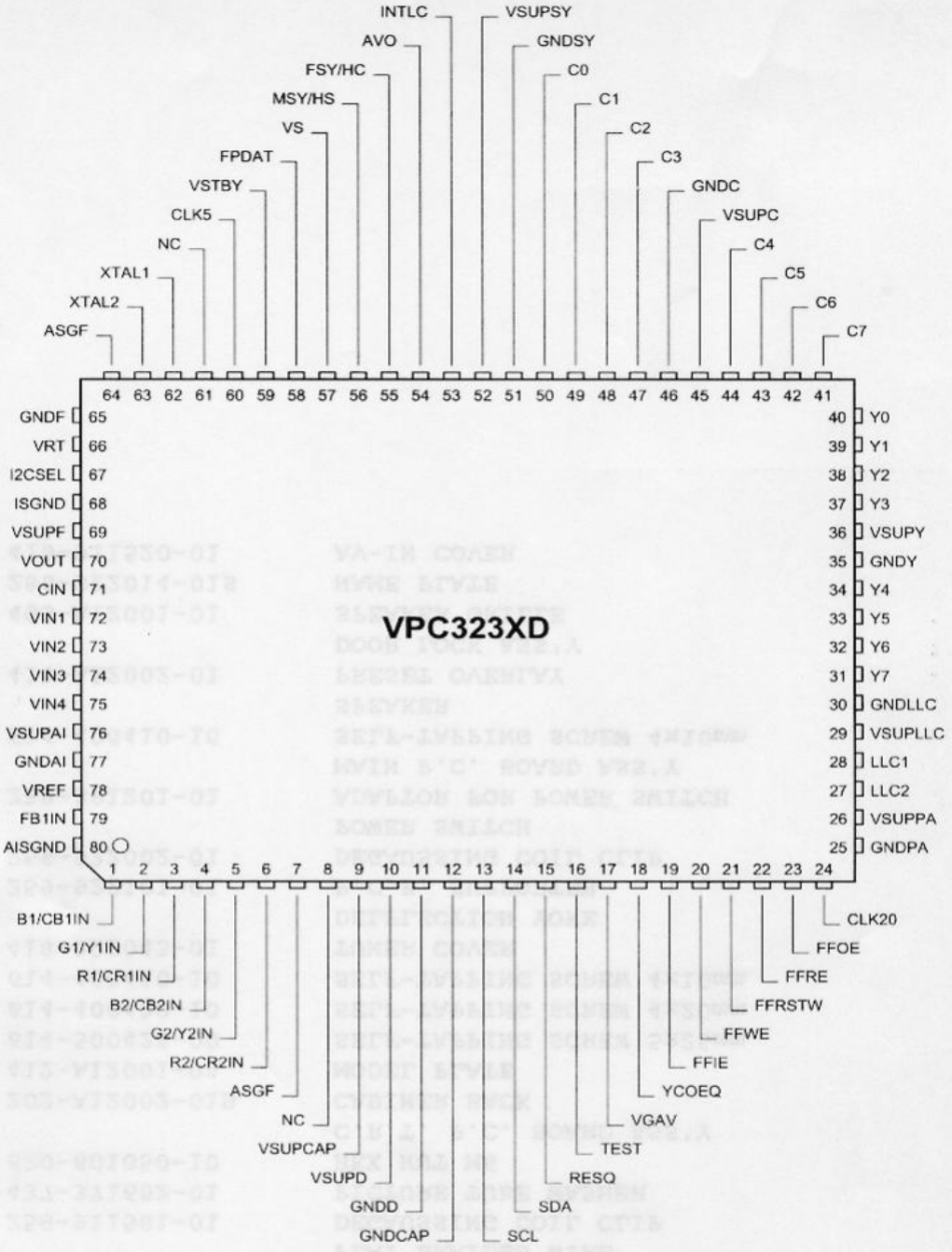


Fig. 4–2: 80-pin PQFP package

TFT LCD Approval Specification

MODEL NO.: V270W1 - L03

Customer: _____

Approved by: _____

Note:

LCD TV Head Division	
Director	許振隆

QRA Dept.	TD Division	DDII	DDI
Approval	Approval	Approval	Approval
陳永一	李汪洋	鈴木優	林文聰

LCD TV Marketing and Project Management Dept.	
Project Manager	胡崇銘、陳立宜

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	August 1,03	All	All	Preliminary Specification is first issued.
Ver 2.0	Sep. 18,03	17	7.2	Contrast ratio:Typ. (600)→600
				Response time T_R:Typ. (15)→15
				T_F: Typ. (10)→10
				Gray to Gray: Typ (16.6)→16.6
				Center Luminance of White: Min. (450)→450
				Typ. (550)→550
				Average Luminance of White: Min. (400)→400
				Typ. (450)→450
				Color Chromaticity Min. Typ. Max. Min. Typ. Max.
				Red Rx (0.616)(0.646)(0.676)→0.616 0.646 0.676
				Ry (0.302)(0.332)(0.362)→0.302 0.332 0.362
				Green Gx(0.239)(0.269)(0.299)→0.239 0.269 0.299
				Gy(0.570)(0.600)(0.630)→0.570 0.600 0.630
				Blue Bx(0.112)(0.142)(0.172)→0.112 0.142 0.172
				By(0.042)(0.072)(0.102)→0.042 0.072 0.102
				Viewing Angle Horizontal θ_x+ Typ. (85)→85
				θ_x- Typ. (85)→85
				Vertical θ_Y+ Typ. (85)→85
				θ_Y- Typ. (85)→85
		5	2.1	Shock (Non-Operating) Max. Value (100)→100
				Vibration (Non-Operating) Max. Value (1.0)→1.0

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V270W1- L03 is a 27" TFT Liquid Crystal Display module with 14-CCFL Backlight unit and 1ch-LVDS interface. This module supports 1280 x 720 WXGA format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is build-in.

1.2 FEATURES

-Ultra wide viewing angle – Super MVA technology

-High brightness (550 nits)

- High contrast ratio (600:1)

- Fast response time

- High color saturation NTSC 75%

- WXGA (1280 x 720 pixels) resolution, true HDTV format.

- DE (Data Enable) only mode

- LVDS (Low Voltage Differential Signaling) interface

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	597.12(H) x 335.88 (V) (26.97" diagonal)	mm	(1)
Bezel Opening Area	603.22 (H) x 341.98 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 720	pixel	-
Pixel Pitch (Sub Pixel)	0.1555 (H) x 0.4665 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-glare with anti-reflective coating Hard coating (2H), Haze: 40% Reflection Rate: < 2%	-	-

1.5 MECHANICAL SPECIFICATIONS

Item			Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)			637.55		mm	Module Size Depth(D)
	Vertical(V)			379.8		mm	
	Depth(D)	W/O INV	-		36	mm	
		W/I INV	40	40.5	41	mm	
Weight			-	4300		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	100	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

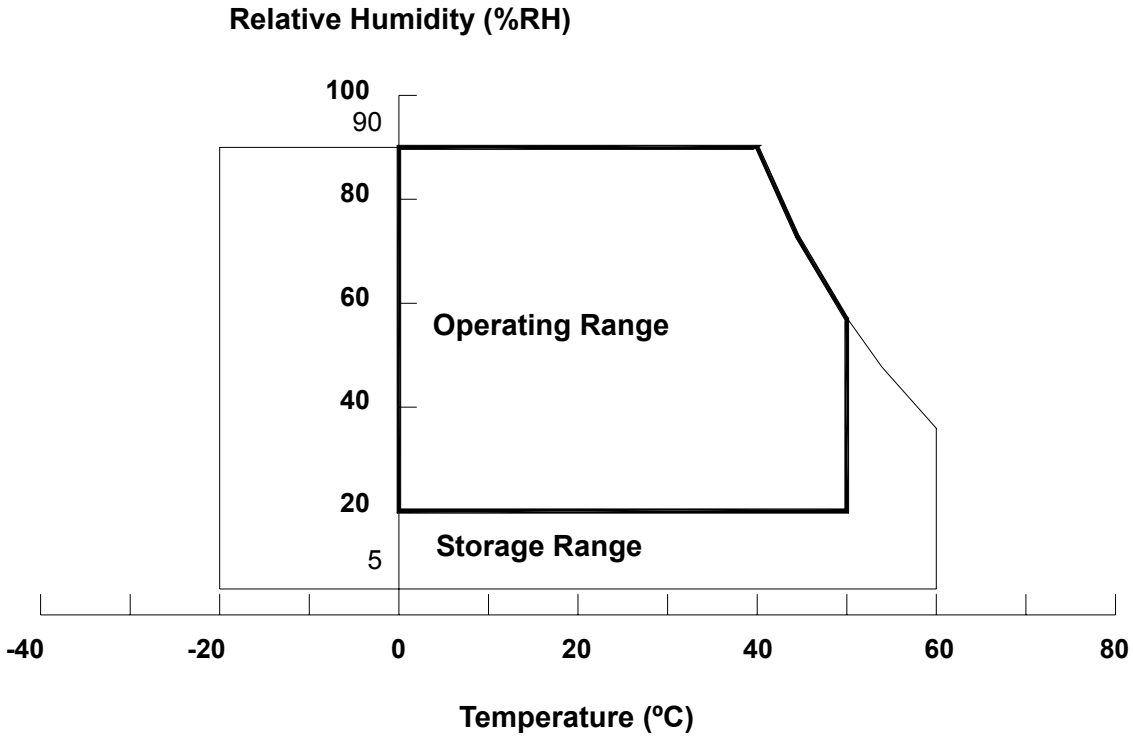
(c) No condensation.

Note (2) The temperature of panel display area surface should be 0 ºC Min. and 60 ºC Max.

Note (3) 2 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 500 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+6.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	4.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbo	Test	Min.	Type	Max.	Unit	Note
Lamp Voltage	V_L	–	0	–	3.0K	V_{RMS}	(1), (2), I_L = 4.7 mA
On/Off Control Voltage	V_{BLON}	–	-0.3	–	7	V	
Internal/External PWM Select Voltage	V_{SEL}	–					
Internal PWM Control Voltage	V_{IPWM}	–					
External PWM Control Voltage	V_{EPWM}	–					
Operating Temperature	T_{OP}	5～95% RH	0	–	75	℃	(3)
Storage Temperature	T_{ST}	5～95% RH	-30	–	80	℃	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

Note (3) Protect inverters from moisture condensation and freezing.

3. ELECTRICAL CHARACTERISTICS

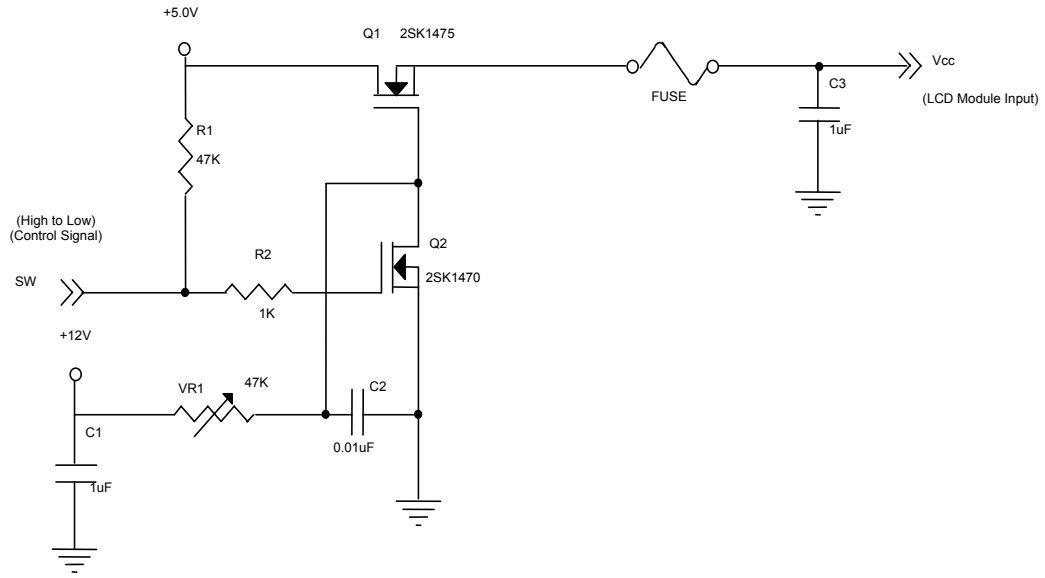
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

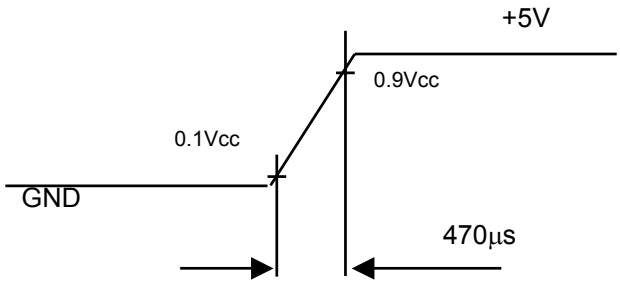
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	4.5	5.0	5.5	V	-
Ripple Voltage		V_{RP}	-	-	200	mV	-
Rush Current		I_{RUSH}	-	2.1	3	A	(2)
Power Supply Current	White	Icc	-	1.4	-	A	(3)a
	Black		-	1	-	A	(3)b
	Vertical Stripe		-	1.2	-	A	(3)c
LVDS differential input high threshold voltage		V_{TH}	-	-	+100	mV	
LVDS differential input low threshold voltage		V_{TL}	-100	-	-	mV	
LVDS common input voltage		Vic	1.125	1.25	1.375	V	
Terminating Resistor		RT	-	100	-	ohm	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at Vcc = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

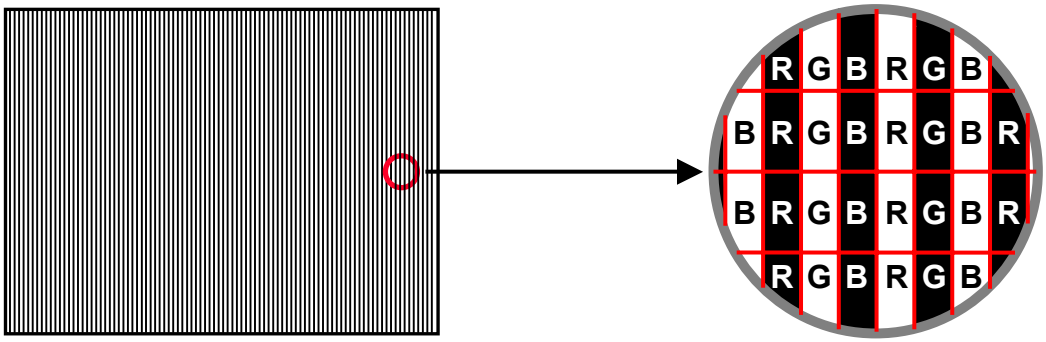
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



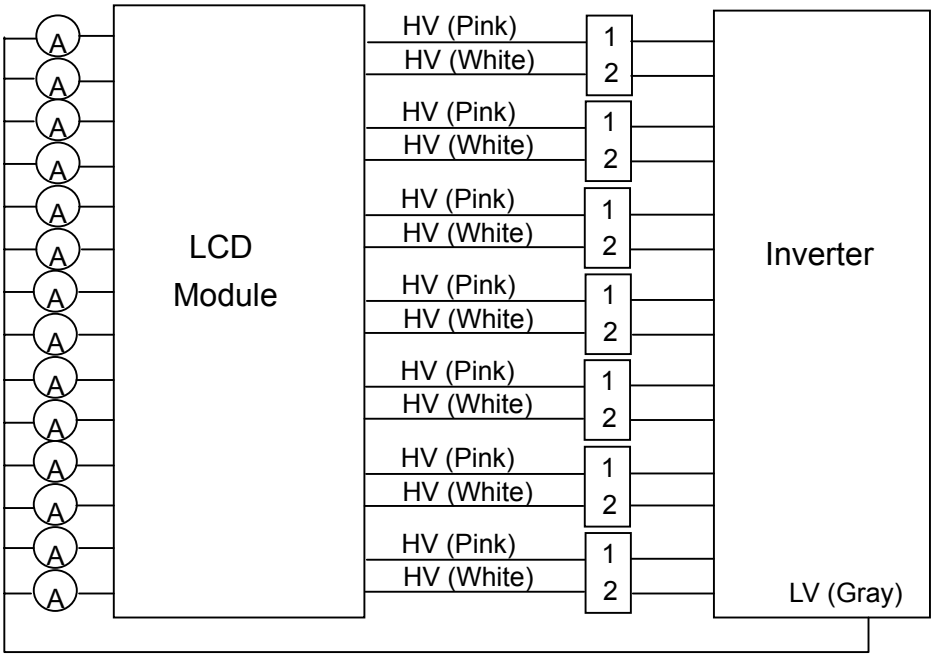
Active Area

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	1008	1120	1232	V_{RMS}	I_L = 4.7 mA
Lamp Current	I_L	4.4	4.7	5.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	1200	-	3000	V_{RMS}	(2), Ta = 25 ºC
		1790	-	3000	V_{RMS}	(2), Ta = 0 ºC
Operating Frequency	F_L	54	56	58	KHz	(3)
Lamp Life Time	L_{BL}	50K	-	-	Hrs	(5)
Power Consumption	P_L	-	92	-	W	(4), Inverter Input

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup.

Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = (\sum_{lamp1-lamp14} I_L \times V_L)/0.8$, P_L is based on the inverter efficiency, which is 80%.

Note (5) The lifetime of a lamp is defined as the time in which it continues to operate under the condition Ta = 25 $\pm$2 ^{o}C and I_L = (4.35) ~ (4.95) mArms until one of the following events occurs:

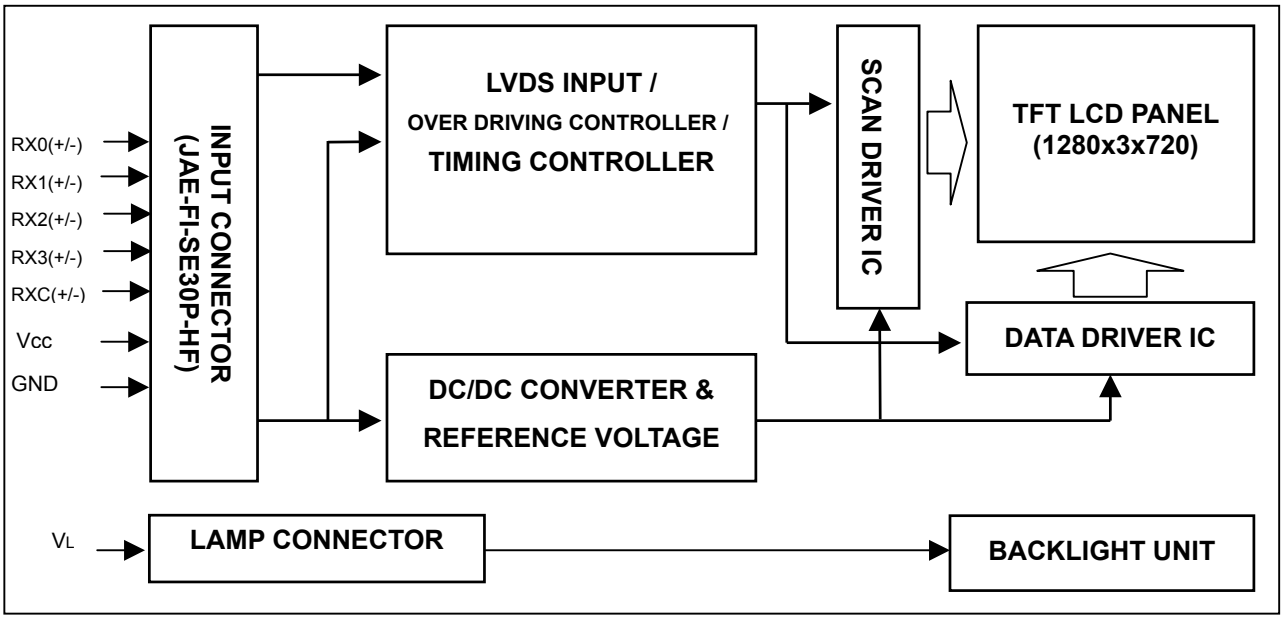
(a) When the brightness becomes equal or less than 50% of its original value.

(b) When the effective discharge length becomes equal or less than 80% of its original value. (Effective discharge length is defined as an area that has equal or more than 70% brightness compared to the brightness at the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE

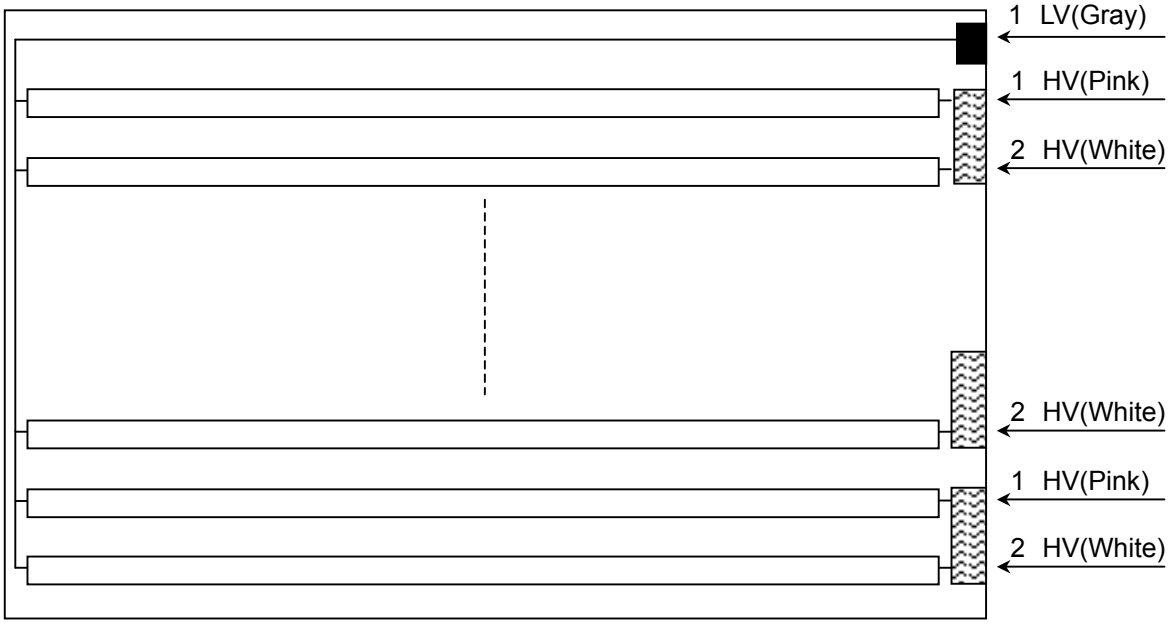


4.2 BACKLIGHT UNIT

Lamp connector

HV : BHR-03-VS-1(JST) *7

LV : ZHR-2 (JST) *1



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Name	Description
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	NC	No Connection
8	GND	Ground
9	RX3+	Positive LVDS differential data input. Channel 3
10	RX3-	Negative LVDS differential data input. Channel 3
11	RXCLK+	Positive LVDS differential clock input.
12	RXCLK-	Negative LVDS differential clock input.
13	GND	Ground
14	GND	Ground
15	RX2+	Positive LVDS differential data input. Channel 2
16	RX2-	Negative LVDS differential data input. Channel 2
17	RX1+	Positive LVDS differential data input. Channel 1
18	RX1-	Negative LVDS differential data input. Channel 1
19	RX0+	Positive LVDS differential data input. Channel 0
20	RX0-	Negative LVDS differential data input. Channel 0
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
I25	GND	Ground
26	VCC	+5.0V power supply
27	VCC	+5.0V power supply
28	VCC	+5.0V power supply
29	VCC	+5.0V power supply
30	VCC	+5.0V power supply

Note (1) Connector Part No.: FI-SE30P-HF (JAE)

Note (2) The first pixel is even.

5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) Connector Part No.: BHR-03VS-1 (JST) or equivalent

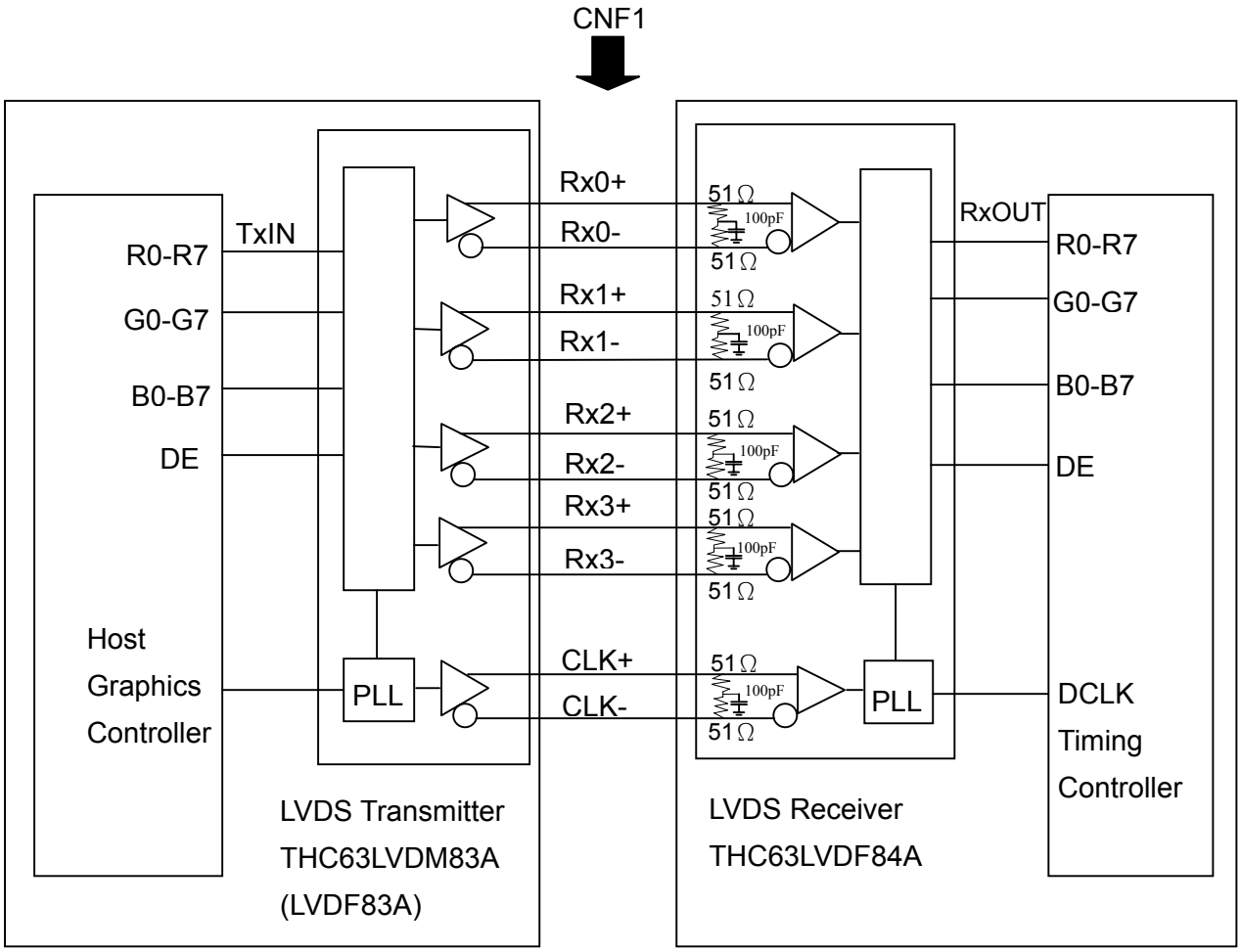
Note (2) User's connector Part No.: SM02(8.0)B-BHS-1TB (JST) or equivalent

Pin	Symbol	Description	Color
1	LV	Low Voltage	Gray
2	NC	No Connection	

Note (1) Connector Part No.: ZHR-2 (JST) or equivalent

Note (2) User's connector Part No.: S2B-ZR-SM3A-TF (JST) or equivalent

5.3 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data
G0~G7 : Pixel G Data
B0~B7 : Pixel B Data
DE : Display timing signal

Notes: 1) The system must have the transmitter to drive the module.
2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0			27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2
	R3	55	TxIN3			32	Rx OUT3	R3
	R4	56	TxIN4			33	Rx OUT4	R4
	R5	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20			54	Rx OUT20	B3
	B4	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26			6	Rx OUT26	DE
	R6	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10			41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
	RSVD 1	25	TxIN23			2	Rx OUT23	Not connect
	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	Not connect
	RSVD 3	28	TxIN25			5	Rx OUT25	Not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Display timing signal

Notes: 1)RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

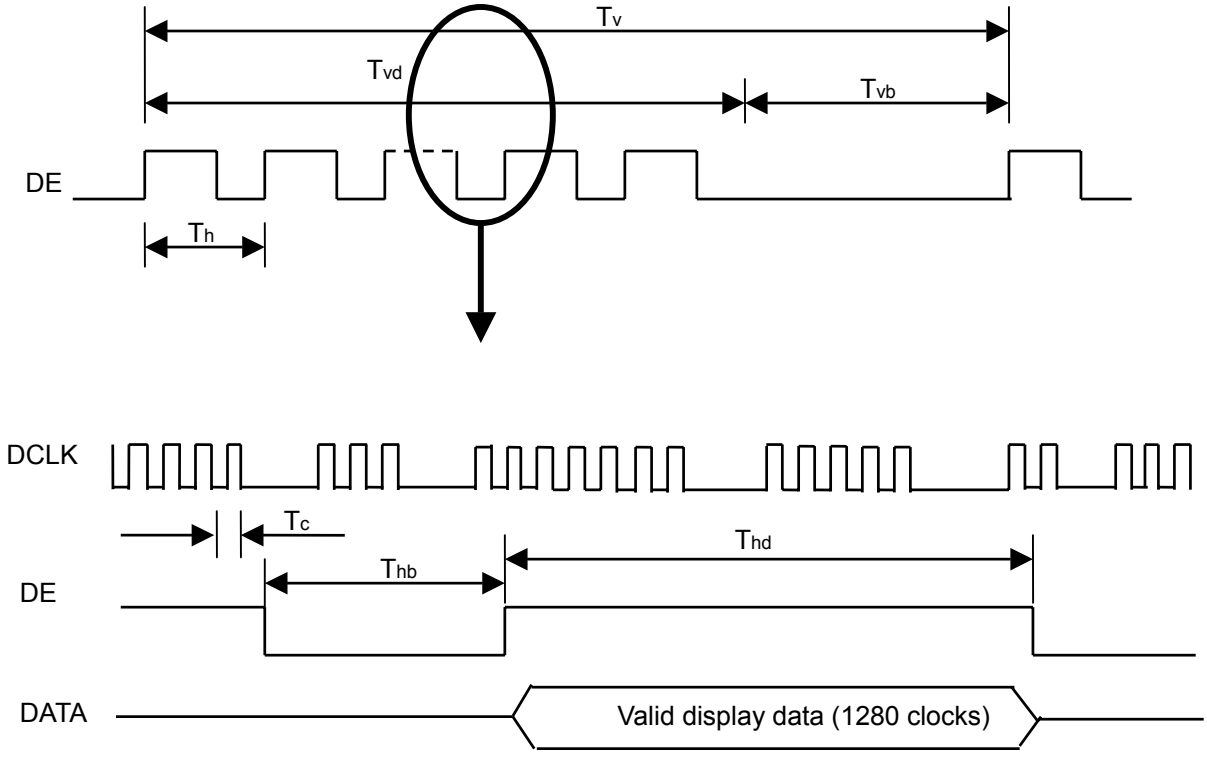
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock	Frequency	1/Tc	70	74.25	80	MHZ	-
Vertical Active Display Term	Frame Rate	Fr	48	60	-	Hz	Tv=Tvd+Tvb
	Total	Tv	730	750	850	Th	-
	Display	Tvd	720	720	720	Th	-
	Blank	Tvb	10	30	130	Th	-
Horizontal Active Display Term	Total	Th	1450	1650	2000	Tc	Th=Thd+Thb
	Display	Thd	1280	1280	1280	Tc	-
	Blank	Thb	170	370	720	Tc	-

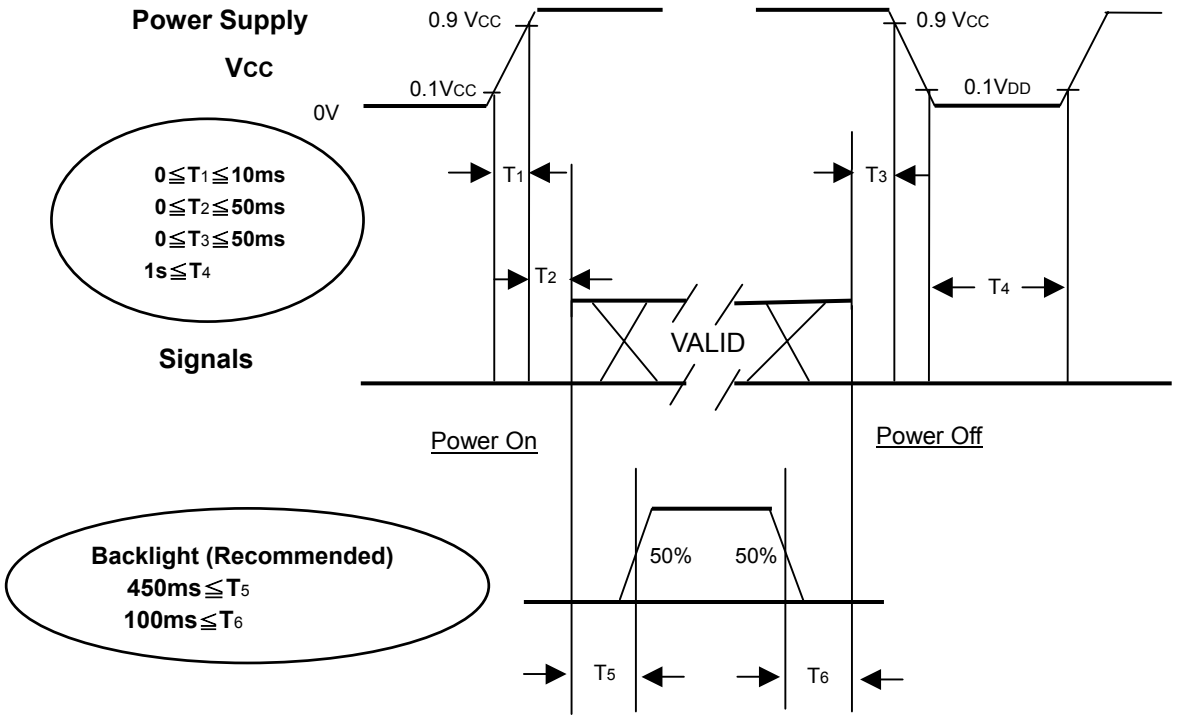
Note: Because of this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	4.7	mA
Inverter Driving Frequency	F_L	56	KHz
Inverter	--		

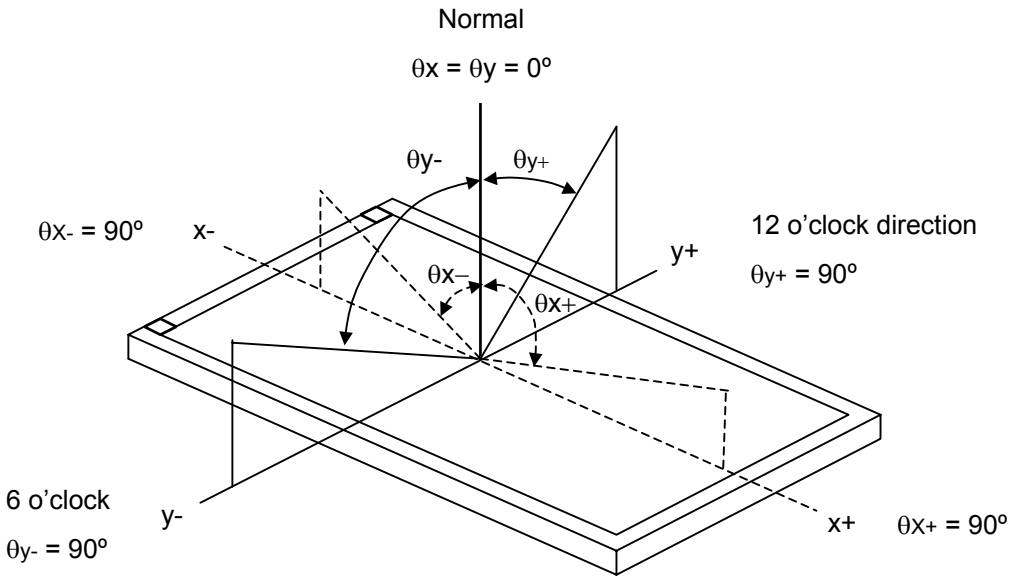
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (7).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	400	600	-	-	Note(2)
Response Time		T_R		-	15	25	ms	Note(3)
		T_F		-	10	20	ms	
		Gray to gray			16.6		ms	Note(4)
Center Luminance of White		L_C		450	550	-	cd/m^2	Note(5)
Average Luminance of White		L_{AVE}		400	450	-	cd/m^2	
White Variation		δW		-	-	1.6	-	Note(8)
Cross Talk		CT		-	-	4.0	%	Note(6)
Color Chromaticity	Red	Rx		0.616	0.646	0.676	-	
		Ry		0.302	0.332	0.362	-	
	Green	Gx		0.239	0.269	0.299	-	
		Gy		0.570	0.600	0.630	-	
	Blue	Bx		0.112	0.142	0.172	-	
		By		0.042	0.072	0.102	-	
	White	Wx		0.255	0.285	0.315	-	9, 300K
		Wy		0.263	0.293	0.323	-	
Viewing Angle	Horizontal	θ_x+	CR≥10		85	-	Deg.	No gray scale inversion
		θ_x-			85	-		
	Vertical	θ_Y+			85	-		
		θ_Y-			85	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

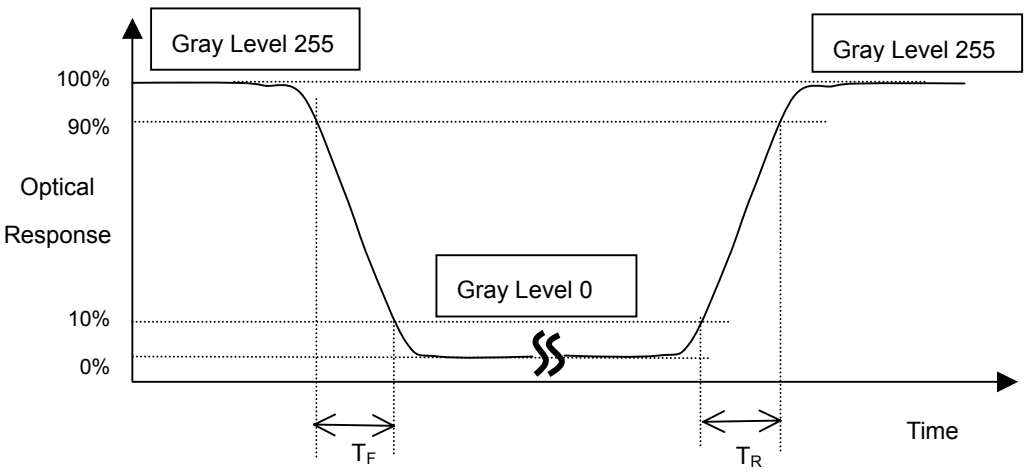
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

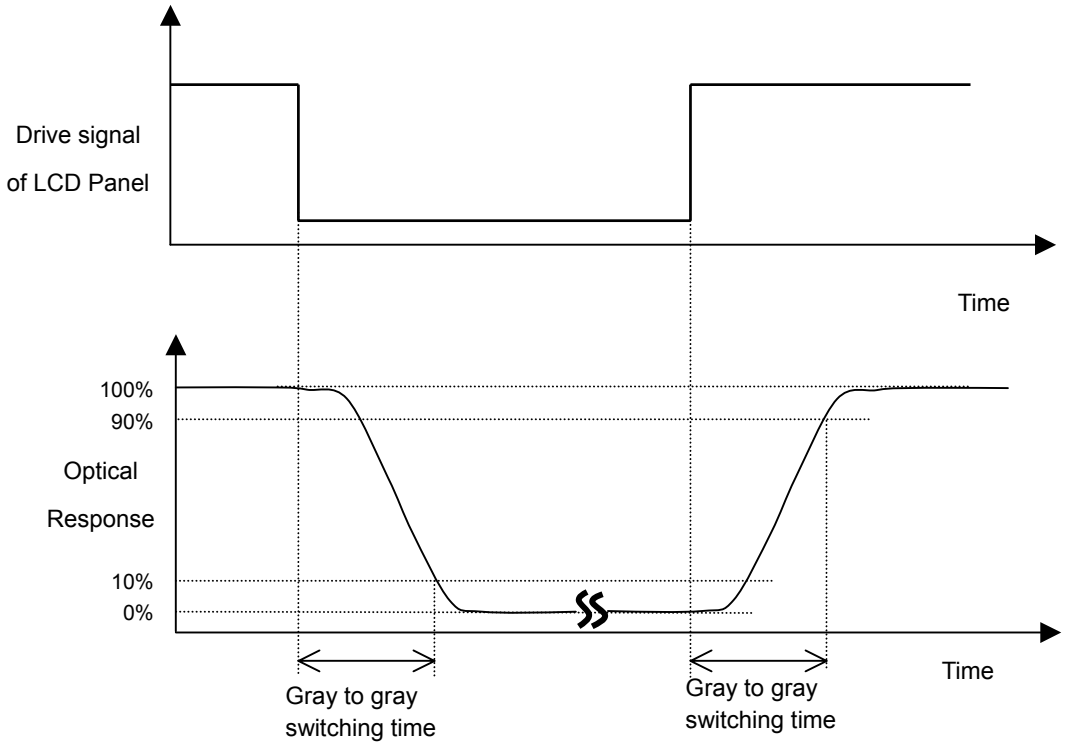
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (8).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0,63,127,191,255.

Note (5) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (8).

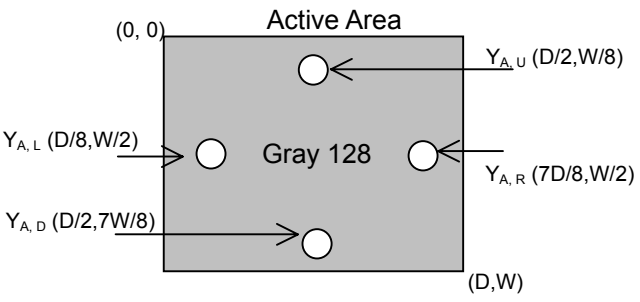
Note (6) Definition of Cross Talk (CT):

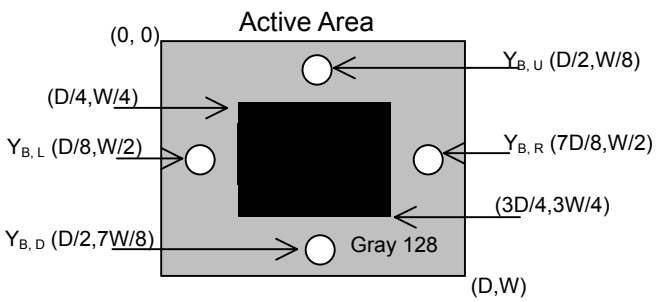
$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

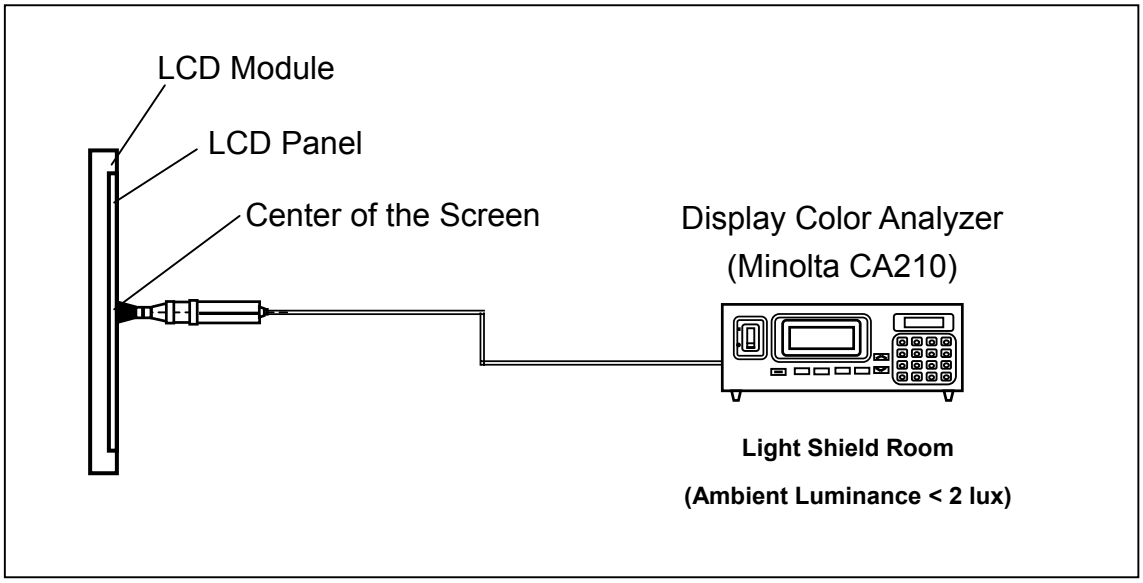
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)





Note (7) Measurement Setup:

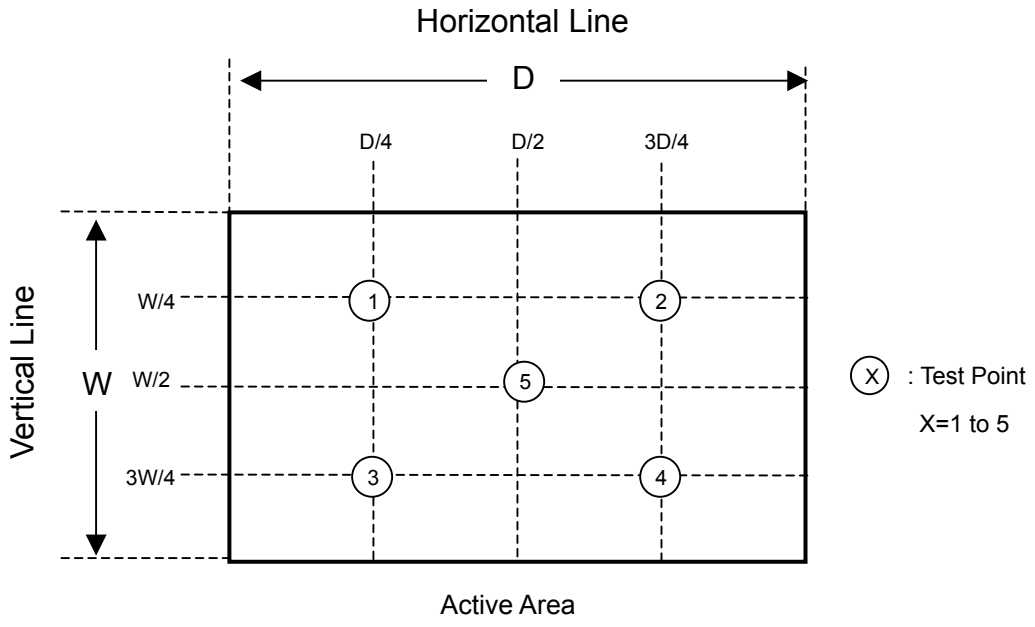
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (8) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PACKAGING

8.1 PACKING SPECIFICATIONS

(1) 4 LCD TV Modules / Carton

(2) Carton Dimensions : 742(L) X 327 (W) X 510 (H)

(3) Weight : Approximately 19Kg (4 Modules Per Carton)

8.2 PACKING METHOD

Figures 8-1 and 8-2 are the packing method

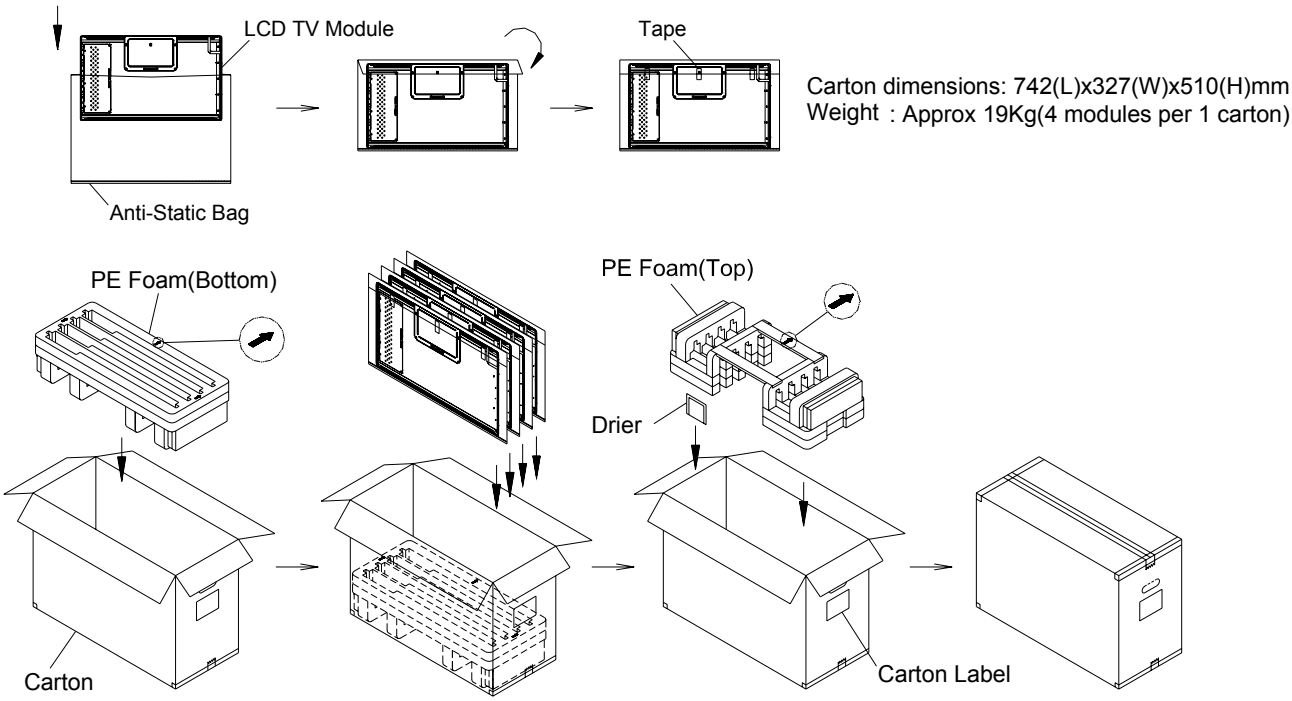


Figure.8-1 packing method

Corner Protector:L1020*50mm*50mm
Pallet:L1100*W1100*H135mm
Bottom Cap:L1100*W1100*H120mm
Pallet Stack:L1100*W1100*H1163mm
Gross Weight:180kg

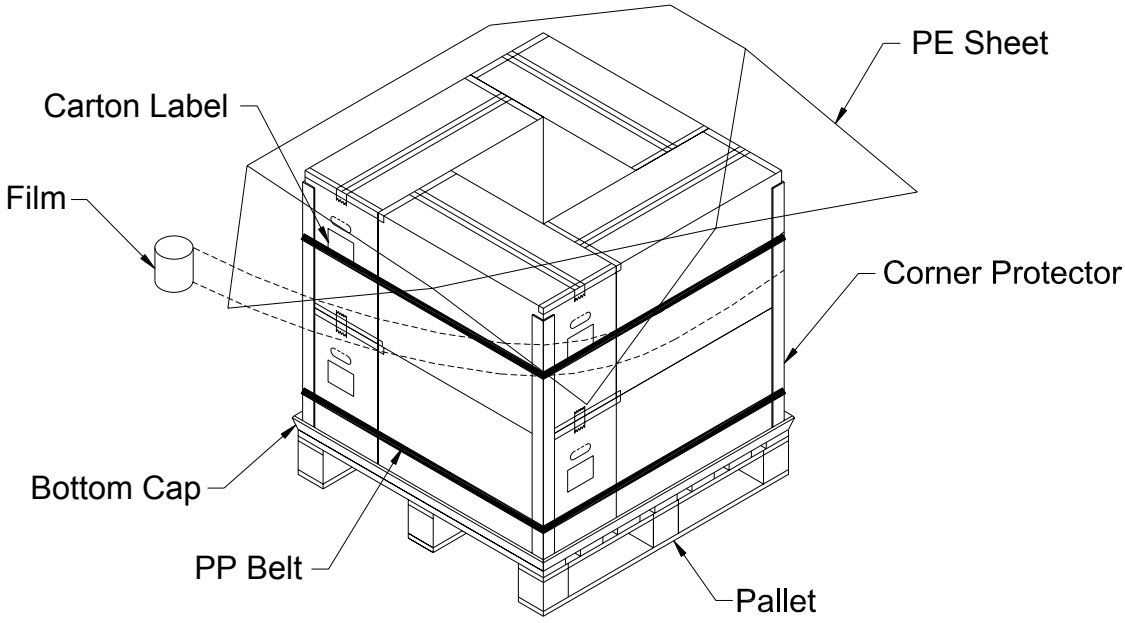
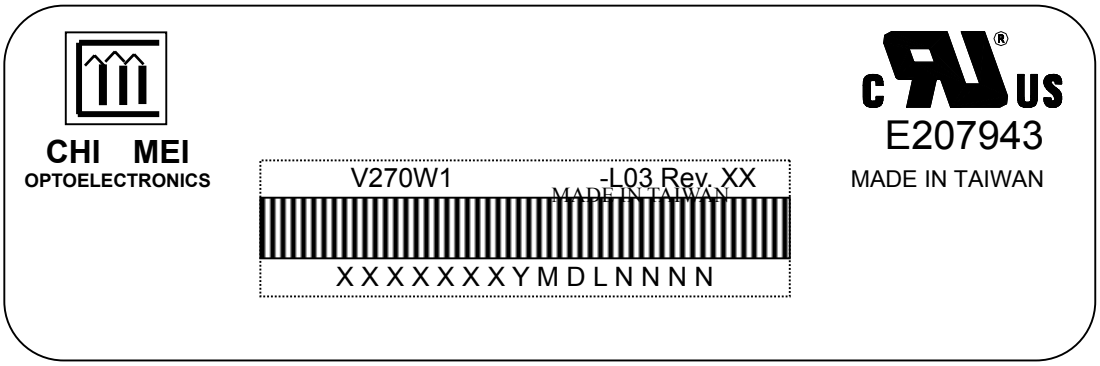


Figure. 8-2 packing method

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

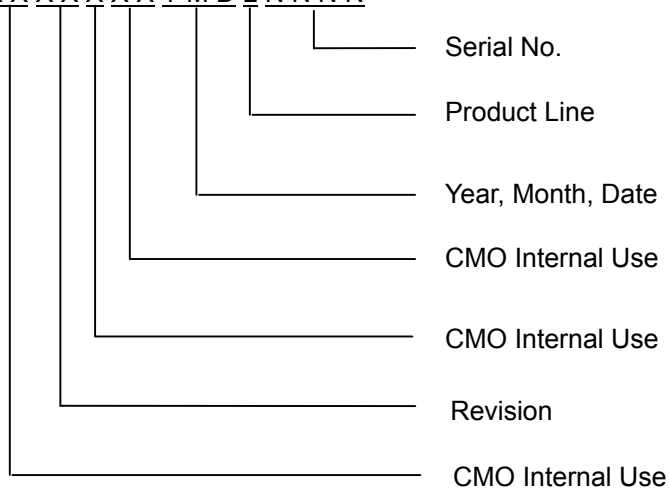
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V270W1-L03

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

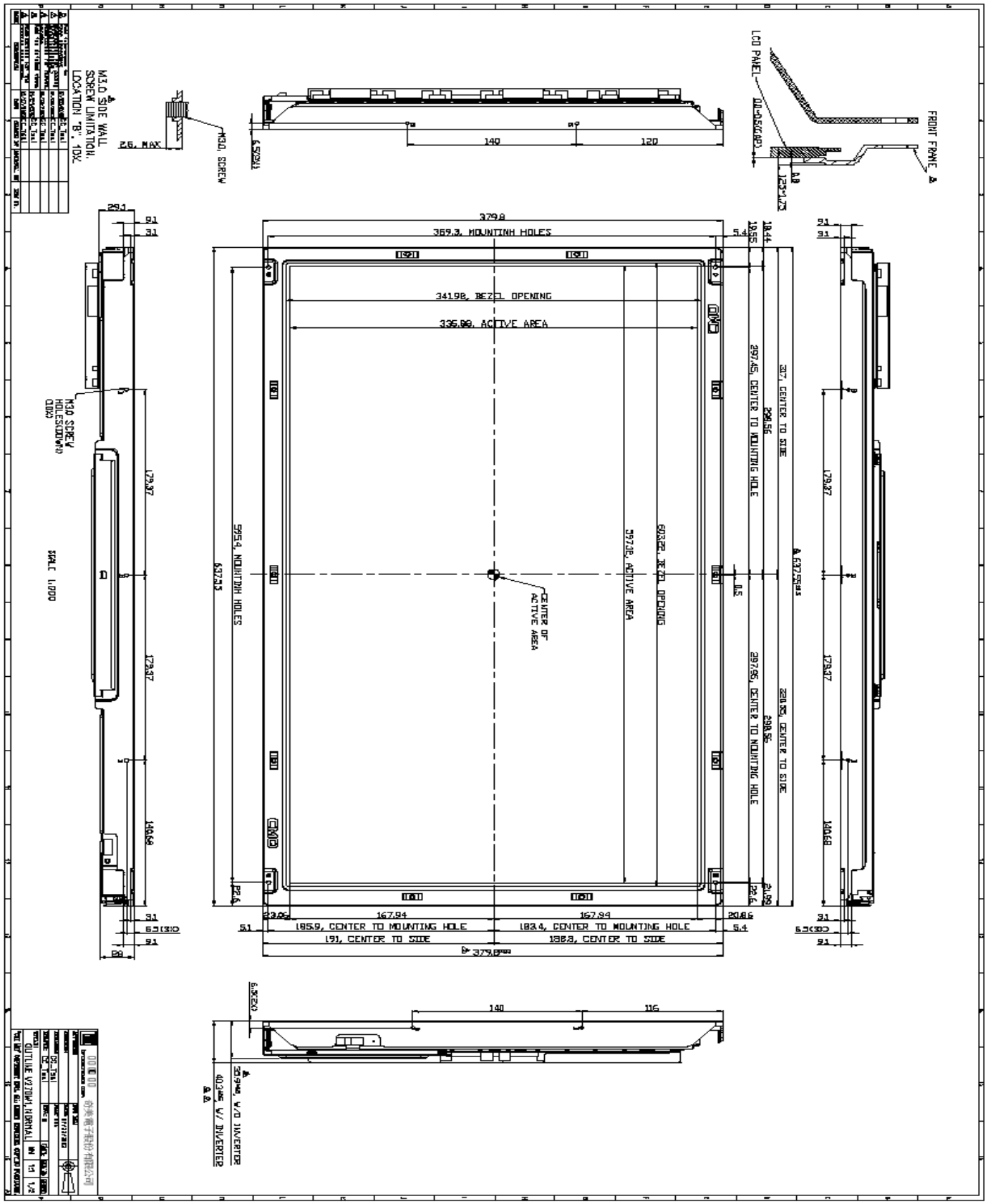
10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

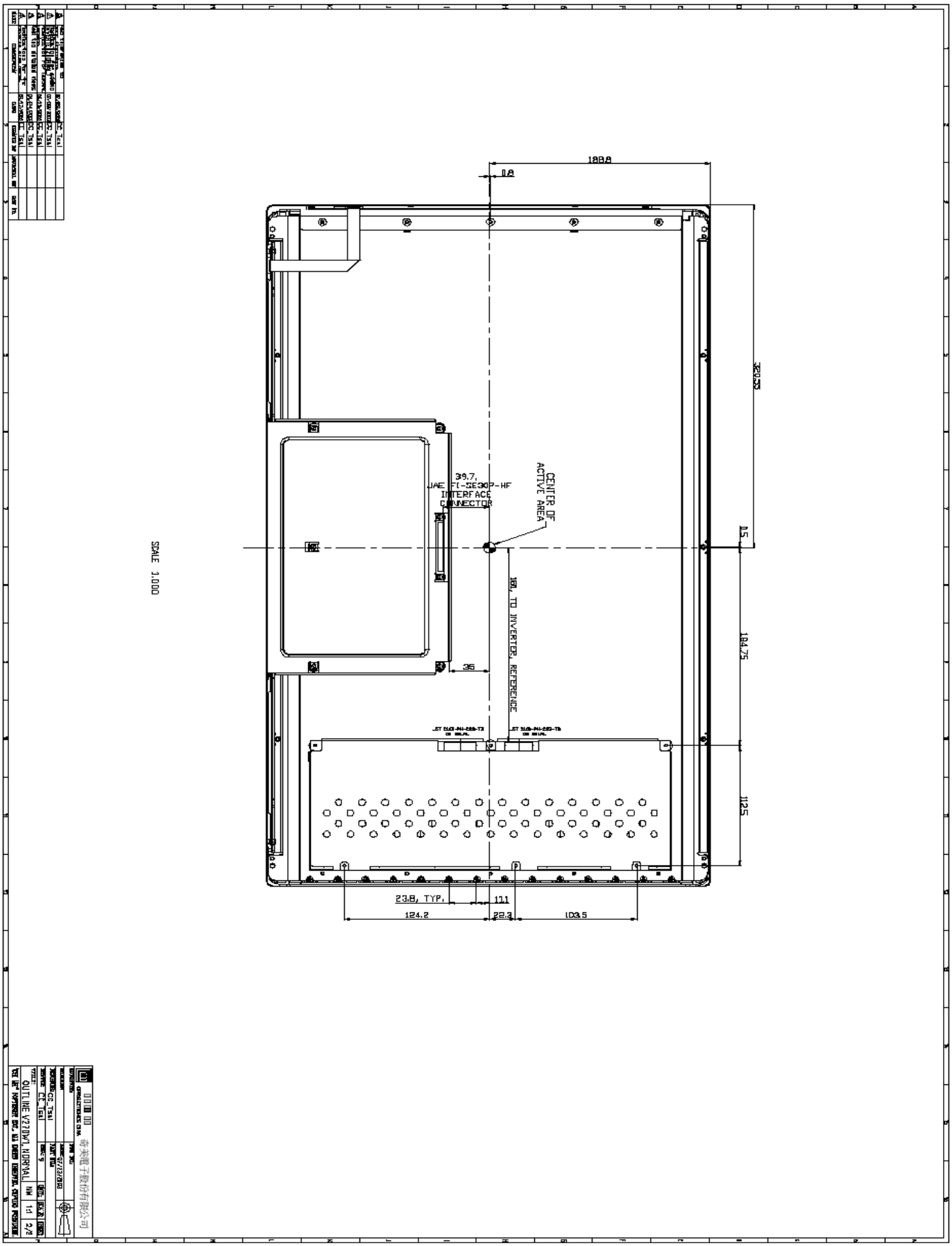
(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

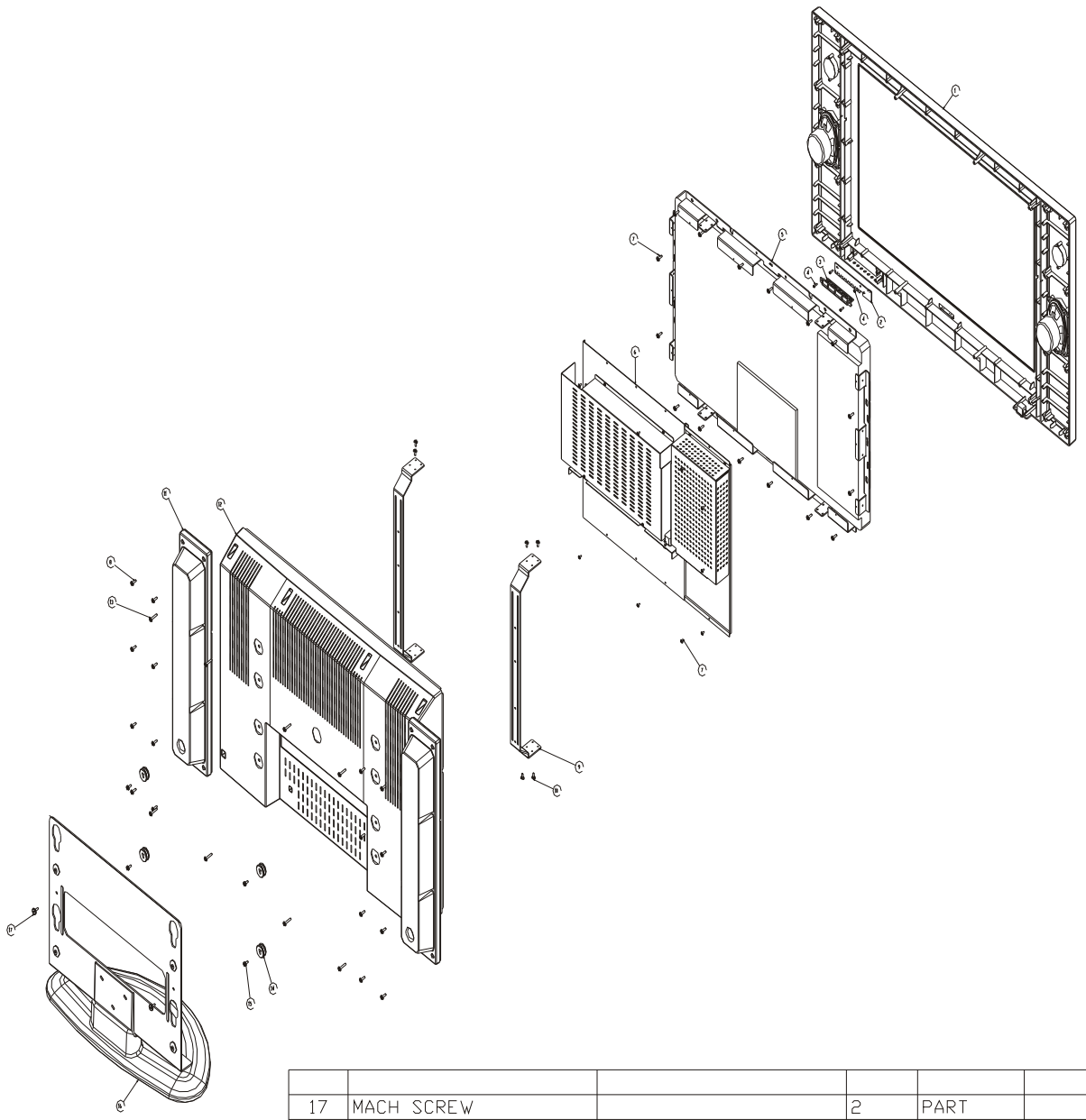
11. MECHANICAL CHARACTERISTICS



 Version 2.0



Exploded View Diagram



17	MACH SCREW		2	PART	
16	SEAT_ASS		1	ASSEMBLY	
-	SOCKET_PVC_PLATE		1	PART	
15	MACH SCREW		4	PART	
14	BKT_1		4	PART	
13	SELF TAPPING SCREW		8	PART	
12	BACK_CAB_26_1		1	PART	
11	SPK_BOX_B1		2	PART	
10	MACH SCREW		8	PART	
9	MTG_BKT_26_2		2	PART	
8	SELF TAPPING SCREW		32	PART	
7	MACH SCREW		9	PART	
6	MAIN_PCB_MTG_ASS_2		1	ASSEMBLY	
5	27PANEL_ASS		1	ASSEMBLY	
4	SELF TAPPING SCREW		4	PART	
3	F_KEY_L26_1		1	PART	
2	KEY_PCB_ASS_26_1		1	ASSEMBLY	
1	FRONT_CAB_ASS_LC27		1	ASSEMBLY	
ITEM	DESCRIPTION	PART NO	QTY.	TYPE	REMARK